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Robust design of high gain amplifiers using dynamical systems and bifurcation theory

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Robust design of high gain amplifiers using dynamical systems and bifurcation theory

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LIST OF SYMBOLS

CMOS: complementary metal oxide silicon
PFA: positive feedback amplifier
VDD: positive supply
VSS: ground node or negative supply
g_m : transconductance
g_o : output conductance
μ: attenuation factor
PVT: process, voltage and temperature
ADC: analog-to-digital converter
DAC: digital-to-analog converter
LSB: least significant bit
MSB: most significant bit
DNL: differential nonlinearity
INL: integral nonlinearity
TT,SS,FF,SF,FS: process corners
TT: typical NMOS with typical PMOS
SS: slow NMOS with slow PMOS
FF: fast NMOS with fast PMOS
SF: slow NMOS with fast PMOS
FS: fast NMOS with slow PMOS
XOR: exclusive or
SOC: system-on-a-chip
FET: field effect transistor
λ : channel-length modulation factor
THD: total harmonic distortion
V_{OS} : offset voltage
HDL: hardware description language
I/Q: in-phase/quadrature
$p(x, y)$: devices' property under gradient influence
Ω: mismatch between two identical devices
FFT: fast Fourier transform

ABSTRACT

High gain operational amplifiers are by far the most fundamental building block in analog and mixed-signal design. In the first few chapters, design of high gain CMOS positive feedback amplifiers (PFAs) is studied. A low-voltage positive feedback amplifier in standard digital CMOS with ≤ 3 transistors stacked between V_{DD} and V_{SS} is designed and circuit details are discussed. With the use of a linear precision MOS voltage attenuator and a digital tuning network, the PFA was simulated to have 100dB DC gain at the operating-point and > 70dB DC gain over a 2Vpp output swing range. Test results of fabricated chips confirmed better than 90dB operating-point DC gain, ≥60dB DC gain over 2Vpp. It has nearly 90 degrees of phase margin and 140MHz gain-bandwidth product when driving 1pF capacitive load with 1mA from 3.5V single supply.

Both linear and nonlinear behaviors of the PFA are carefully studied in order to enhance and maintain high gain automatically. Inherent nonlinearity in its DC transfer curve is discovered and analyzed. Based on nonlinear dynamic systems and bifurcation theory, we predict bifurcation and hysteresis phenomena in the PFA. An algorithm, which can be implemented using simple digital logic, is developed to measure the PFA's open-loop stability as the bifurcation parameter changes. Parameter-tuning algorithms are constructed that systematically move the amplifier's operational point towards the bifurcation point, at which infinite DC gain happens. In order to compensate for the PFA's high sensitivity to process and temperature variations, flexible analog design integrating digital programmability and inexpensive and adaptive digital post-processing techniques are developed. This flexibility and post-processing capability could dramatically enhance the

PFA's yield. Full corner simulation results over wide temperature range verify the bifurcation phenomena and the effectiveness of the control algorithms. It is shown that this amplifier can maintain high performance in the most advanced digital CMOS technology at very low voltage supplies. They also demonstrate that the proposed approach offers a robust PFA design with both high yield and high performance.

Matching of critical components is the most fundamental property that is necessary in achieving high linearity performance of analog mixed-signal circuits. Although matching qualities in future advanced digital CMOS technology are forecast to deteriorate as feature sizes continue to shrink, there has not been significant progress in developing advanced matching layout strategies. Chapter 4 is devoted to addressing this issue. In this chapter, systematic mismatch error in integrated circuits due to gradient effects is modeled and analyzed. Three layout strategies with improved matching performance are proposed and summarized. The hexagonal tessellation pattern can cancel quadratic gradient errors with only 3 units for each device and has high area-efficiency when extended. Both the N^{th}-order circular symmetry patterns and N^{th}-order central symmetry patterns can cancel up to N^{th}-order gradient effects between two devices using 2^N unit cells for each one. Among these three techniques, the central symmetry patterns have the best-reported matching performance for Manhattan structures; the circular-symmetry patterns have the best theoretical matching performance; and the hexagonal tessellation pattern has high density and high structural stability. The N^{th}-order central symmetry technique is compatible to all IC fabrication processes requiring no special design rules. Simulation results of these proposed techniques show better matching characteristics than other existing layout techniques under nonlinear gradient effects. Specifically, two pairs of P-poly resistors using 2^{nd} and 3^{rd}-order central

symmetry patterns were fabricated and tested. Less than 0.04% mismatch and less than 0.002% mismatch were achieved for the 2nd and the 3rd-order structures, respectively. Our proposed new layout strategies improved matching performance significantly.

CHAPTER 1. GENERAL INTRODUCTION

1.1 Introduction

Designing amplifiers, bias circuits, modulators, references, oscillators, analog filters, analog phase-locked-loops and data-converters belongs to analog circuit design. Both analog design and digital design have evolved from discrete to integration, both used different semiconductor materials, and both achieve great successes in MOS integration technology. Nowadays, analog integrated-circuit design dominates the area of analog circuit design and analog design is referred to analog integrated-circuit design. Analog design essentially includes circuits design and test. Because of the dominance of MOS technology, MOS analog design has become the most prevalent work.

MOS technologies have advanced as Moore's Law [1] predicted during the past four decades, which leads to higher integration densities, finer feature sizes and lower supply voltages. Exponential feature size shrinkage served as the main driver for semiconductor development. However, this traditional scaling has nearly reached its fundamental limit [2].

Recently, international technology roadmap for semiconductors (ITRS) identified three system-drivers supporting future semiconductor development: high-volume custom-microprocessor unit (MPU), analog/mixed-signal (AMS), and system-on-chip (SOC) [2]. Mixed-signal/analog design plays a critical role in all these three system drivers: high-speed digital design is colligated to mixed-signal/analog design; AMS is directly related to mixed-signal/analog design; part of a SOC can be associated with mixed-signal/analog design. A mixed-signal SOC requires both high performance digital part and high performance analog

part. Integrating analog functions in SOC is the trend and low cost is a key issue to achieve success.

1.2 Difficulties in Analog Design

Although mixed-signal/analog design plays so important roles in future semiconductor development, ITRS identified it as a difficult challenge and a bottleneck due to the following reasons.

- Decreased supply voltage
- Increased Interference between analog and digital blocks
- Reduced testability
- Increased parametric variations
- Limited design productivity and skills

- Difficulty 1: decreased supply voltage

In designing analog functions in MOS technology, circuit designers are forced to use the technology chosen for the digital part of the circuit. For the classical analog design, supply voltage determines the maximum achievable signal level. Decreasing supply voltage reduces available signal power. Over the past four decades, feature size shrinking in digital CMOS is the basis for the development of semiconductor [1]. This shrinking reduces the supply voltage, which makes analog design tough. Because experts in semiconductor industry lack of good solutions, ITRS recommended using high supply voltage for analog devices [2]. As mentioned in ITRS, this method is not effective while expensive, and does not simplify design effort. When high supply voltage is used for analog circuits, special processing steps have to be added in the digital processes to keep analog devices reliable.

Typically, such actions will reduce the benefit introduced by feature-size shrinking greatly. Realizing high performance analog functionalities using the same digital supply voltage is still demanding for low-cost, high-performance and reliable analog/mixed-signal circuits and systems.

- Difficulty 2: increased interference between analog and digital blocks

In mixed-signal design, both analog supply and digital supply coexist on the same chip and both analog part and digital part share the same bulk. Signal coupling through substrate and interconnect is a serious issue in mixed-signal circuits as well as in high-speed applications [3, 4, 5]. Interference from digital supply to analog supply is another issue in mixed-signal circuits. Most high precision analog/mixed-signal circuits and systems require a stable supply. However, it is a nontrivial task, especially when more and more transistors are integrated in a smaller chip with feature size shrinking.

- Difficulty 3: reduced testability

Because of the trend of continuously higher integration, internal nodes are increasingly more difficult to reach. Design for test (DFT) and built-in-self-test (BIST) for analog/mixed-signal integrated circuits become a necessity [2, 6]. Traditional analog design lacks DFT and BIST techniques. Analog circuits are typically characterized using high precision stimuli and high-resolution measurement. Researchers are naturally thinking of transplanting these accurate stimuli and measurement on a chip and modifying their designs to enable these on-chip tests [7]. However, accurate characterization of analog circuits is a challenging task even with the highly accurate testers whose value is in a few million of US

dollars. Integrating these high precision analog stimuli and high-resolution measurement on a chip is dauntingly expensive and nearly impossible. Testing requirements for future analog circuits call for the evolution of new analog design, which requires only low-precision stimuli and low-resolution measurements [8].

- Difficulty 4: increased parametric variations

ITRS has also indicated "increasing relative parametric variations" another most daunting mixed-signal challenge. These variations were once known as process variations. With the shrinking of feature size in CMOS technology, fabrication process becomes more complex. This has increased process variations. ITRS suggested "active mismatch compensation and tradeoffs between speed and resolution". Post-processing on designed-redundancy is an effective way to compensate process variations. Traditional analog/mixed-signal design uses sliding-contact, Zener Zapping, fusible links and laser trimming techniques to calibrate the fabricated chips so the calibrated chips will get better performance under calibration environment [9]. Because of the randomness of process variations, theoretically, every chip should be calibrated separately. In product test and calibration procedure, a few chips in a wafer are first calibrated separately and then the average calibration pattern is applied to the whole wafer or even a whole run to reduce test-calibration cost. Most of these methods require expensive testers and special calibration tools. Because semiconductor devices are highly temperature related, analog circuits is sensitive to temperature variations. In order to measure circuits' performances at different temperatures, test engineers use oven to emulate the application environments. This procedure is time-consuming and expensive. In order to limit test and post-processing cost, industry typically calibrates the analog/mixed-signal circuits in the most convenient test

environment. Analog/mixed-signal circuits' performance can deviate a lot if the application conditions are far away from the testing conditions.

Digital calibration techniques have been successfully used in mixed-signal circuits such as data converters within high supply voltages [10, 11, 12, 13, 14]. It shows economic advantages over traditional trimming and fuse based post-processing techniques. However, not much research efforts on digital post-processing have resulted in practical solutions to enhance analog/mixed-signal circuits' performance. *Lack of economic solutions in low-voltage applications* remains a key obstacle.

- Difficulty 5: limited design productivity and skills

Traditional analog design was considered as an art instead of a scientific technique. It is more of an experience-based than knowledge-based approach. Circuit designers use trial-and-error way to design high performance analog circuits, which requires special expertise and lots of time gaining such experiences. This approach increases design cost exponentially when a new technology is introduced. ITRS has identified "shortage of design skills and productivity" as one of the most daunting mixed-signal challenges. Without bringing new design methodologies, the shortage of design skills and productivity will continue to increase because of the high standard and cost for engineers entering this area.

1.3 High Gain Amplifier Design in Low-Voltage Digital CMOS

Amplifier design, the most fundamental analog design, can illustrate the huge impact of technology advancement and the imminent requirement for innovative combination of diverse science knowledge.

The monolithic operational amplifier (op amp) is by far the most widely known and used analog circuit and analog building block in analog/mixed-signal systems, including continuous-time filters, switched-capacitor amplifiers, delta-sigma modulators, pipeline ADCs, DACs and other countless applications. Since its introduction in the mid 1960s, the monolithic op amp has proliferated into many different designs. The MOS op amp designs have become the most important building blocks of analog circuits because of the fast advancement of MOS fabrication technologies.

1.3.1 Key performance indexes of an amplifier

An amplifier has several key performance metrics: DC gain, gain-linearity, gain-bandwidth-product, phase-margin, power consumption, common-mode rejection ratio (CMRR) and so on. Among these parameters, DC gain, gain linearity and gain-bandwidth-product and power consumption are in our interest.

- DC gain

An ideal op amp has an infinite DC gain while a practical op-amp can approximate the ideal op-amp well in low frequency [9]. DC gain, a key index of the op-amp, plays a critical role in high precision systems. For example, DC gain determines gain error in a switched capacitor amplifier, and this determines the final settled signal accuracy [15]. The amplifier in a pipeline ADC stage plays a critical role for the available ADC performance. High resolution ADC requires a high gain amplifier to limit performance degradation introduced by gain error [16].

- Gain linearity

Open loop gain linearity determines available signal/distortion ratio in close-loop configured amplifiers. Most circuit designers were directly mapping open-loop gain

nonlinearity to close-loop nonlinearity and thus were reluctant to use high gain highly nonlinear amplifiers in pipeline stages, for fear of poor performance for total harmonics distortion (THD) and spurious-free dynamic ratio (SFDR). However, high open-loop gain helps to reduce signal distortion in close loop configurations [16].

- Gain-bandwidth product(GB) and power consumption

GB reflects how fast the op-amp can operate. In switched capacitor amplifiers, this parameter indicates how fast the charge can be transferred to the output. GB is directly related to power consumption.

1.3.2 High gain amplifier structures

Telescopic cascode, folded cascode, regulated cascode amplifiers have successfully realized both high DC gain and large output swings at large feature size with high supply voltages [15]. However, these traditional amplifier structures have failed to maintain both high gain and large output swings simultaneously at the advanced CMOS technologies due to dramatically reduced supply voltages. A telescopic or folded cascode structure can maintain moderate gain; however, it cannot provide sufficiently large output swings [15]. A multi-stage cascade structure with simple differential stages can provide large output swings; however, the structure is unfavorable because of the degradation of frequency-response due to complex compensation [15]. Positive feedback structures have the potential to provide low-voltage compatibility, large output swings and good frequency responses simultaneously [17, 18, 19, 20, and 21]. However, it is sensitive to process and temperature variations and yield tends to be much less than other kind of amplifiers.

1.3.3 Focus of our research

Our research aims at enhancing the positive feedback amplifier's gain and yield over process, voltage and temperature variations through different calibration schemes with the help of nonlinear system dynamical theories.

1.4 Thesis Organization

In addition to this introduction, this thesis consists of 5 more chapters. Chapter 2 discusses a single-stage positive feedback amplifier (PFA) suitable for driving capacitive feedback. It utilized an adjustable linear MOS attenuator in the positive feedback path which provided stable negative-conductance cancellation over wide process-supply voltage-temperature (PVT) variations. Simulations suggested it achieved greater than 80dB DC gain and test results confirmed this for all fabricated amplifiers. Chapter 3 illustrated nonlinear bifurcation phenomenon in the PFA and its application in automatically calibrating the PFA to its highest performance despite large PVT variations. This would solve the major limit in the PFA-- improving yield. This chapter is expanded from "Robust design of high gain amplifiers using dynamical Systems and bifurcation theory" [26, 27]. In this chapter, we introduced a two-loop binary search algorithm to automatically and efficiently search the optimal feedback factor. Our new algorithm is based on bi-state detection with pull-up pull-down methods. In analog/mixed-signal design, matching is the most critical property to achievable performance. Three new layout techniques are developed and good matching is obtained. Chapter 4 summarizes these results. In chapter 5, the relationship between open-loop nonlinearity and close-loop linearity was quantitatively investigated. This chapter is expanded from "Equivalent gain analysis of nonlinear operational amplifier" [16] and its

deduction is fully proven by thorough theoretical derivations. Chapter 6 concludes this dissertation.

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CHAPTER 2. A POSITIVE FEEDBACK AMPLIFIER IN DIGITAL CMOS

Chengming He, Degang Chen, Randall Geiger

Abstract

A low-voltage positive feedback amplifier in standard digital CMOS with ≤ 3 transistors stacked between V_{DD} and V_{SS} is presented and circuit details are discussed. With the use of a linear precision MOS voltage attenuator and a digital tuning network, the PFA was simulated to have 100dB operating-point DC gain. Test results of fabricated chips confirmed better than 90 dB operating-point DC gain, ≥ 60dB DC gain over 2 Vpp output swing. It has nearly 90 degrees of phase margin and 140 MHz gain-bandwidth product when driving 1 pF capacitive load with 1mA current from a single 3.5 V supply.

I. Introduction

For the past four decades, the semiconductor industry has advanced as Moore's Law predicted [1]. The advances in CMOS process technologies have pushed the feature sizes below 90nm [2] and reduced supply voltages significantly to ensure reliability. However the threshold voltages for digital transistors have not decreased as quickly as supply voltages because of the need to avoid large-scale leakage. Such changes impose significant challenges to analog circuit design, in particular to designs of high-gain, large output, swing amplifiers [3]. Cascoding and multi-stage cascading are two traditional design solutions for high-gain amplifiers. With more than 4 transistors stacking from VDD to VSS, cascoding is not

suitable for low-voltage applications with large output swing requirements. Though cascading is compatible with low voltage, its frequency response is often degraded too much by complex compensation. Positive-feedback technique and negative conductance cancellation has been shown to be an effective alternative to achieve high DC gain with good frequency response while also achieving the potential of low-voltage supply applications [4 , 5]. However, most positive feedback structures rely heavily on matching, which makes it dauntingly difficult to maintain performance over process and temperature variations. Furthermore, most positive-feedback amplifiers show strong nonlinearity in the form of sharp gain decreases as the output swing becomes large. Efforts have been made to decrease the gain dependence on output swing [6].

This paper describes a fully differential positive feedback amplifier with an internal positive attenuation feedback. Fully differential structure provides both positive and negative outputs, which make it easy to generate negative conductance. The attenuator uses solely MOS devices while providing high attenuation that is insensitive to process-supply temperature variations, making one design variable highly controllable. This geometric ratio-dependent precision MOS attenuator also helps decrease gain sensitivity to output swing. The amplifier stacks a maximum of only 3 transistors between VDD and VSS, which makes it well suited for low-voltage applications. Single-stage configuration has an inherent advantage in frequency response, stability, settling speed, and power efficiency in achieving the required gain-bandwidth product. A high DC gain over the full output swing range is achieved with the help of a digital tuning network. Test results confirmed the design and simulation results.

Section II discusses the new positive-feedback amplifier architecture and circuit details. In Section III, simulation results are discussed and test results are presented. Section IV summarizes the outcome of the research project.

II. Amplifier Structure and Circuit Detail

2.1 Proposed positive feedback amplifier

Fig. 1 shows the concept of conductance-cancellation amplifier. It consists of a transconductance (g_m) cell and a resistive load of $-R_2$ in parallel with R_1. It can be shown that this amplifier has a gain

$$A = -g_m \frac{R_1 R_2}{R_2 - R_1} = \frac{g_m}{g_1 - g_2}, \quad (1)$$

and the gain will reach infinity if g_2 is equal to g_1.

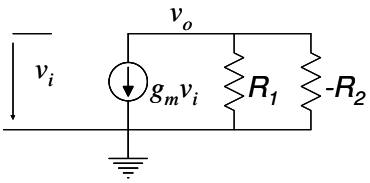
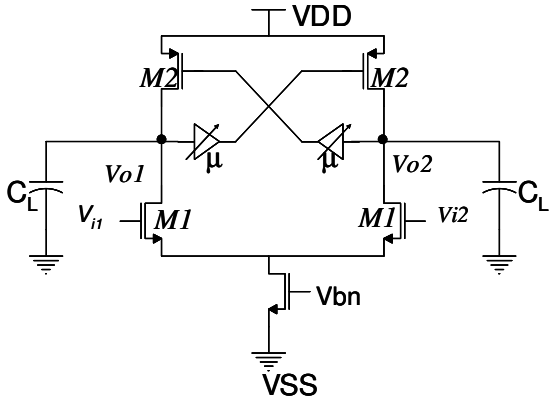


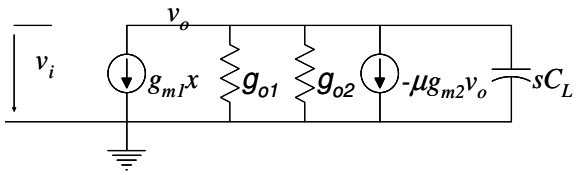
Fig. 1 concept of negative conductance cancellation

Practically, fully differential structure provides a simple solution to realize negative conductance since it has complementary outputs. Fig. 2 shows the basic architecture of the proposed positive feedback amplifier (PFA). Equation (2) can be derived using small-signal-equivalent circuit analysis for the differential signal path with denoting $v_o = v_{o1} - v_{o2}$ and $v_i = v_{i1} - v_{i2}$

$$\frac{v_o}{v_i} = -\frac{g_{m1}}{sC_L + g_{o1} + g_{o2} - \mu g_{m2}}. \tag{2}$$



(a)



(b)

Fig. 2 a) proposed positive feedback amplifier; b) small-signal equivalence

Define

$$\mu_0 = \frac{g_{o1} + g_{o2}}{g_{m2}}, \tag{3}$$

this suggests the positive feedback amplifier will achieve an infinite DC gain when $\mu = \mu_0$ while μ is less than 1.

2.2 Precision MOS attenuator

2.2.1 Active linear NMOS voltage divider

Fig. 3 displays an active linear NMOS voltage divider first proposed by Kim [7]. Equation (4) expresses its attenuation factor,

$$k = 1 - \sqrt{1-\theta} \quad \text{and} \quad \theta = \frac{W_2 / L_2}{W_1 / L_1 + W_2 / L_2}. \tag{4}$$

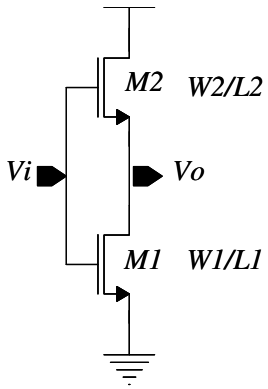


Fig. 3 an active linear NMOS voltage divider

The attenuator shown in Fig. 3 provides some interesting properties. Parameter θ is a geometric ratio that does not scale with processes and can be well controlled by layout. The attenuation *k* is only dependent on geometric ratio θ, thus it could be made extremely precise. In addition, this voltage divider has infinite DC impedance at its input, which will not change the operating-point of the main amplifier.

2.2.2 Proposed programmable precision MOS attenuator

Fig. 4 shows the proposed precision MOS attenuator consisting of three cascading voltage dividers. The first stage is composed of M1 and M2, the second of M3 and M4 (PMOS), while the third stage consists of M5 and M6. The total attenuation is expressed in (5)

$$\mu = k_1 k_2 k_3 . \tag{5}$$

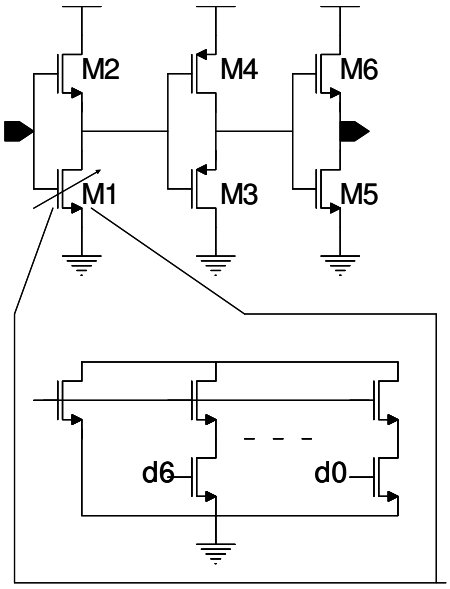


Fig. 4 precision MOS Attenuator

Cascading structure provides not only quiescent operating-point shift but also appropriate biasing for the MOS transistors that generate negative conductance. Furthermore, total attenuation μ is allocated in three stages with scaled-up attenuations, which reduces sensitivity to process variations. This was confirmed by simulations.

2.2.3 Digital programmability and quantitative analysis

Previous studies have shown that the positive feedback amplifier is sensitive to process and temperature variations. In order to overcome these variations, the internal feedback should have sufficient adjustment range and provide convenient external control. This adjustment range is PVT dependent, which can be obtained by corner simulations. Denote this range as (6)

$$[\mu_{0\min}, \mu_{0\max}]. \tag{6}$$

Ideally, continuous adjustment is preferred in order to maintain infinite DC gain over PVT variations. However, discrete control with digital logic provides robustness and simplicity while maintaining sufficient performance in most applications. Theoretically, a N1-bit binary-weighted DAC provides 2^{N1} possible attenuation values. Defining Γ to be the equivalence of input codes and Δ the LSB of the DAC (assuming Δ>0), the ideal attenuation μ can be expressed as (7)

$$\mu = \mu_m + \Delta\Gamma. \tag{7}$$

In order to assure the design has sufficient tuning range, the attenuator must meet certain specifications depending on the desired amplifier DC gain. According to (2), (3) and (7), the amplifier gain can be rewritten as (8)

$$A = \frac{g_{m1}}{[\mu_0 - (\mu_m + \Delta\Gamma)]g_{m2}}. \tag{8}$$

Equation (9) shows that the optimal control code for the maximum DC gain falls in

$$\Gamma_1 = \left\lfloor \frac{\mu_0 - \mu_m}{\Delta} \right\rfloor, \quad or \quad \Gamma_2 = \left\lceil \frac{\mu_0 - \mu_m}{\Delta} \right\rceil. \tag{9}$$

For the sake of simplicity, g_{m1}/g_{m2} can be approximated to be 1. Thus the lower bound DC gain of the positive feedback amplifier could be estimated as

$$A \geq 1/\Delta . \tag{10}$$

2.2.4 Design specifications for the attenuator DAC

Given the above analysis (equation 6-10), it is feasible for a designer to discover the specifications for the attenuator DAC. To achieve certain yield over PVT, three conditions must be met: sufficient coverage (11), fine resolution (12), and required DAC size (13):

$$\mu(\Gamma = 0) < \mu_{0\min} < \mu_{0\max} < \mu(\Gamma = 2^{N1}), \tag{11}$$

$$\varepsilon_{\mu} = \max_{0 \leq \Gamma \leq 2^{N1}-1} \{\mu(\Gamma+1) - \mu(\Gamma)\} \leq \Delta = \frac{1}{A_{spec}}, \tag{12}$$

$$2^{N1} \geq \frac{\mu_{0\max} - \mu_{0\min}}{\Delta} . \tag{13}$$

The sufficient coverage condition (11) is solely related to the required adjustment range (6). Although, one can argue for the use of equal sign in both lower and upper bounds, the more stringent and conservative inequality sign was imposed for the sake of simplicity.

The fine-resolution condition (12) places a stricter requirement on the DAC DNL, while equation (13) determines the minimal DAC size. For a very high desired DC gain A_{spec} and wide adjustment range, the DAC design could become nontrivial. However, for realistic gain requirements, e.g., 80dB minimum, the necessary adjustment range is quite modest. This makes the DAC design a relative easy task. For example, in the AMI-0.5um process, simulation results show that a simple 6-bit DAC with LSB=0.00007 is sufficient. In order to leave some design margin, a 7-bit DAC was integrated into the precision MOS attenuator.

2.2.5 Attenuator DAC linearity and attenuation sensitivity to PVT

Fig. 5 illustrates the total attenuation with different DAC control codes. Notice that monotonicity of the DAC is well maintained and DNL/INL is also reasonably low. Though, as will be demonstrated late, the linearity performance of the DAC is noncritical.

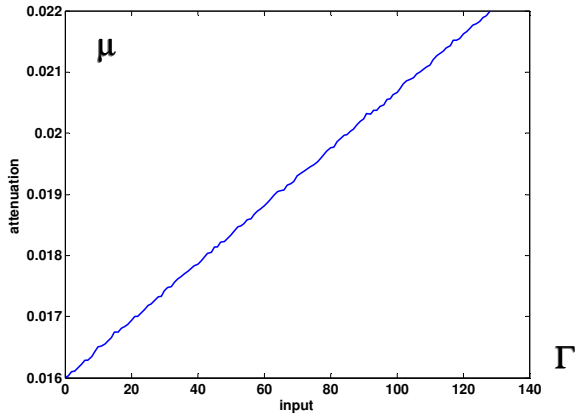


Fig. 5 attenuation versus DAC codes

Fig. 6 shows the attenuator's strong insensitivity to supply voltage. As a result, in the first order approximation the effect of supply variation on the attenuator can be ignored.

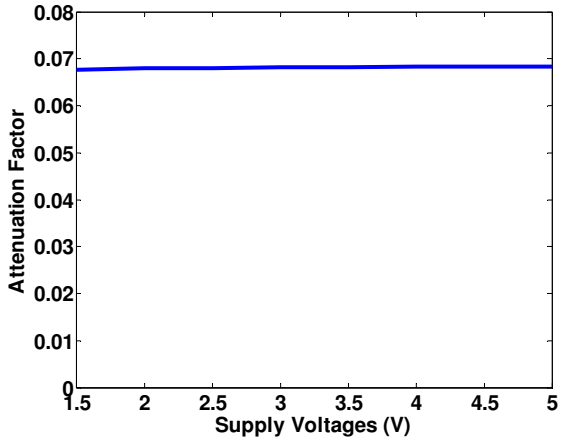


Fig. 6 attenuation sensitivity to supply change

III. Simulation Results

The proposed amplifier shown in Fig. 2 was simulated over process (TT, SS, FF, SF and FS), supply (3.0-4.0V) and temperature (0-100°C) variations. More than 80dB DC gain was simulated with appropriate selection of digital control codes. For the typical corner in particular, DC gain of 110 dB was achieved with an optimal 7-bit control code at room temperature (shown in Fig. 7).

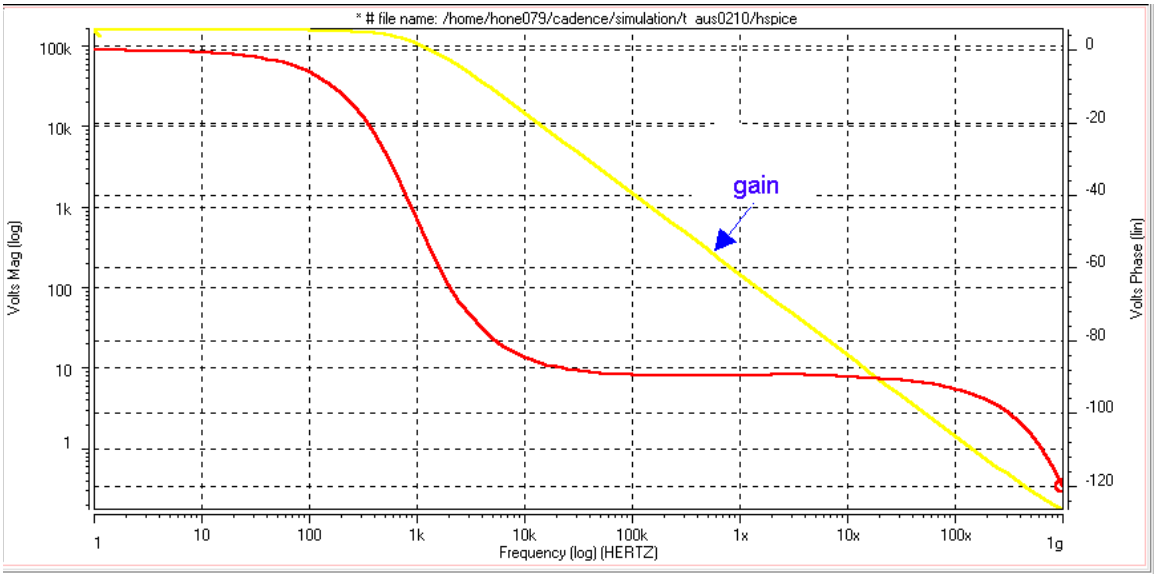


Fig. 7 AC response of the single-stage, positive-feedback amplifier

Simulations also verified that temperature would affect the amplifier's performance. With a fixed control code obtained at a certain temperature, the amplifier gain performance degrades as operating temperature varies. Thus, in-field recalibration is preferred. Fig. 8 shows the DC gain over wide temperature range with and without temperature compensation. Temperature compensation (or re-calibration) helps maintain performance.

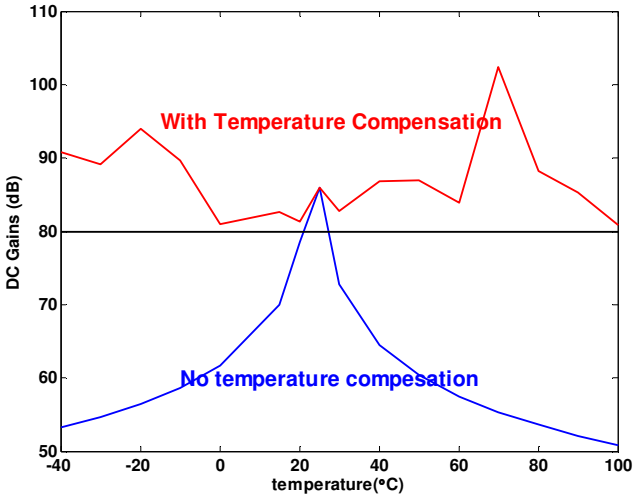


Fig. 8 DC gain with temperature variations

The effect of selecting an incorrect control code on performance was also studied. Fig. 9 displays the gain sensitivity to control-codes. With a fixed control code, the DC gain dropped quickly as the output swing increased. However, when the control code was adjusted accordingly, more than 85dB DC gain was maintained over an output swing range of 2Vpp.

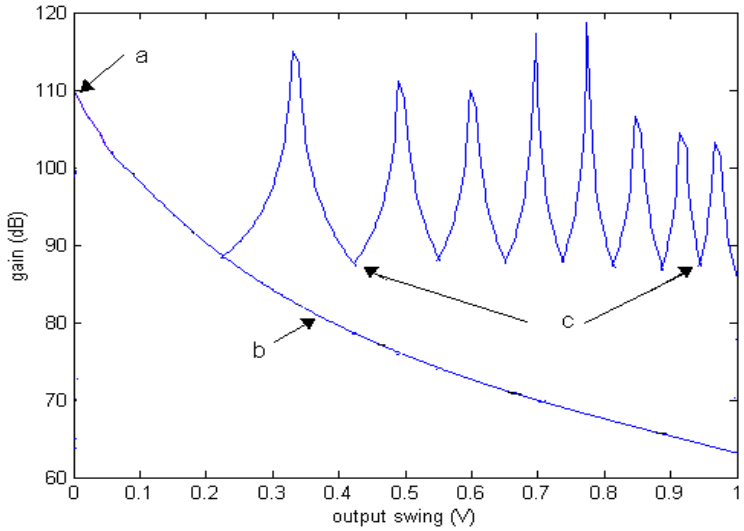


Fig. 9 simulated amplifier DC gain versus output swing (with/without adjusting attenuation)

IV. Layout and Fabrication

Matching of analog circuits is critical for performance. Common-centroid and symmetric layout techniques are widely adopted in analog circuitry for parameter matching and thermal balance. For this project, the PFA core was selected for fabrication. Layouts of all transistors were drawn carefully, as shown in Fig. 10. Its input NMOS pair and negative-conductive PMOS pair fully explored common-centroid technique, while biasing current NMOS uses multi-finger structure with source/drain sharing technique. Input pair and load pair are placed in two different guard-rings to improve signal isolation.

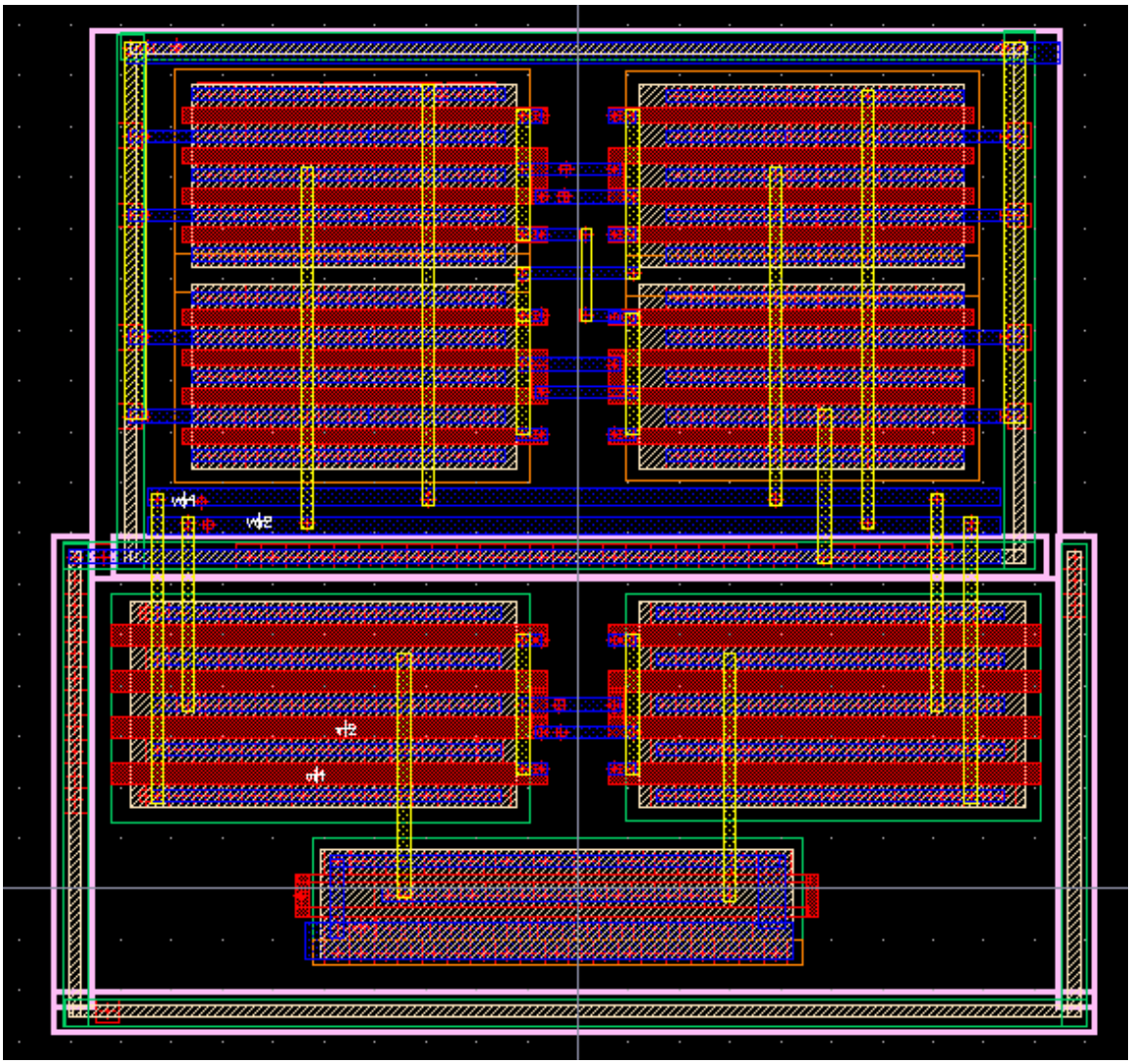


Fig. 10 common-centroid layout within guard-rings

The internal feedback pair was placed as close as possible in a center-symmetric way. These techniques help obtain good matching.

Fig. 11 shows the fabricated amplifier through the MOSIS education program including PADS. Its core area is 280um*120um. This amplifier was designed, simulated, and fabricated with an AMI 0.5um digital CMOS process.

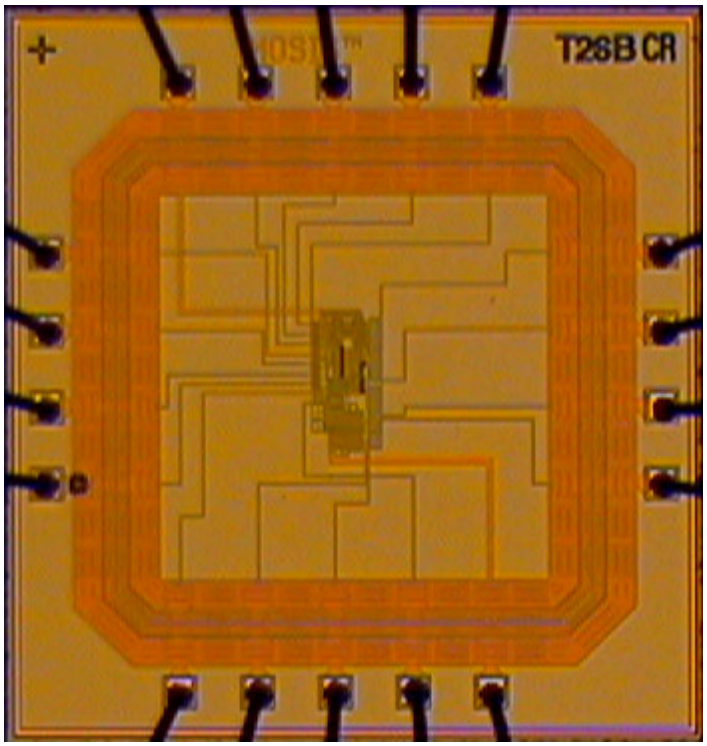


Fig. 11 Die photo of the fabricated amplifier with auxiliary circuits

V. Testing/Tuning and Measurement

With capacitive loads in the output, the main pole of the open-loop amplifier may vary from negative to positive depending on the attenuation factor μ. Theory of linear systems indicates that a system is stable if all poles are in the left half-plane, and that the system becomes unstable if any pole moves into the right half-plane. Because positive feedback can cause one or more open-loop poles of an amplifier to move into the right half-plane, traditional wisdom in IC design has led designers to avoid positive feedback amplifiers. Such caution is unjustified since an Opamp is never intended to be used in open-loop and closed-loop stability can be easily guaranteed with appropriate feedback [8].

That the open-loop stability of the amplifier can be changed from stable to unstable with different levels of positive feedback motivates a tuning strategy for this positive feedback amplifier. Recall that the positive feedback factor is directly controlled by the attenuator factor μ, which is in turn controlled by a small tuning DAC. Gradually changing the DAC input code can cause the amplifier's dominant open-loop pole to move from the left half plane into the right half plane. Because of this, an optimal DAC input code will cause the amplifier open-loop pole to be closest to the origin. When this happens, the amplifier's DC gain reaches maximum. Also when the amplifier's dominant pole changes sign, the DC gain of the amplifier also changes sign. Therefore, the input-output relationship changes from "in phase" to "phase inversion". This change of "in-phase" can be used as an indicator that the control DAC's input code has changed from small to large, allowing a determination of whether the optimal code has been identified. Due to process variations, each amplifier will have a different "optimal code" at a certain operating point. The phase inversion detection [8, 9] technique can be used during testing to capture the individual optimal code.

5.1 Phase inversion detection

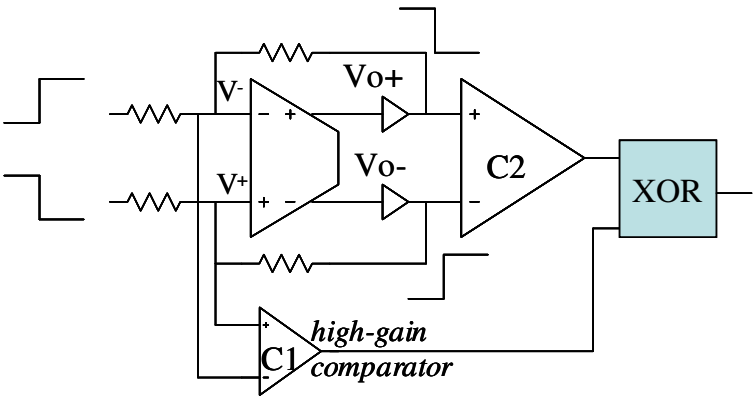


Fig. 12 phase inversion concept

Fig. 12 shows the basic idea of phase inversion detection. It consists of the amplifier core, two buffers, resistive feedback network, one high-gain comparator C1 and one low-gain comparator, C2, as well as a digital XOR-gate.

As shown in equation (1), the DC-gain could be either positive or negative. When the amplifier is configured in a close loop, the feedback network can be easily designed to make the loop stable. Depending on the stability of the open-loop amplifier, polarity of the input could be either as the same as the output or opposite to the output. This can be explained using equation (14) for low-frequency signals:

$$V^+ - V^- = \frac{V_o^+ - V_o^-}{A}. \tag{14}$$

When a square wave is inserted into the input, the output will also be in square wave. If the open-loop amplifier is stable, phase of the internal input $V^+ - V^-$ will be opposite to the output. Otherwise, both are in-phase. This property is illustrated in Fig. 13. These waveforms can be used to indicate the amplifier's open-loop stability.

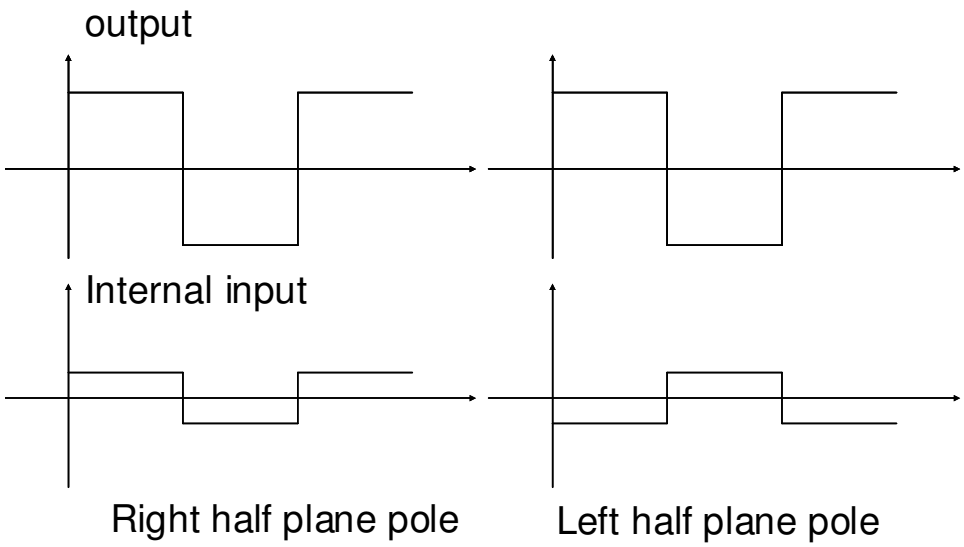


Fig. 13 input/output waveforms with pole locations

The waveforms shown in Fig. 13 are for illustration purpose and are not drawn in proportion. In fact, the input signal is very weak due to high gain of the amplifier under test. A high-gain comparator (C1) amplifies the weak signal and helps to determine the polarity.

As shown in Fig. 12, a low-gain comparator (C2) also digitalizes the output signal. Two comparator's outputs (in digital level) indicate the pole location of the amplifier. '1', given by the XOR gate, indicates right-half plane poles, while '0' implies left-half plane poles. Accordingly, '1' indicates a need to reduce the internal feedback μ while '0' means larger μ is needed. Thus, the best control code Γ_{opt} for the optimal feedback factor μ_{opt} would be located after a few steps of such comparison. Assuming the DAC attenuator has good INL/DNL, both linear searching and binary searching methods are feasible. If this function can be realized using logic control, a positive-feedback amplifier with automatic gain enhancement will be realized.

5.2 Challenges in the phase inversion detection technique

Theoretically, phase-inversion detection provides a ready solution to determine the amplifier's open-loop pole location. However, as shown in Fig. 13, a major challenge is designing the high gain comparator C1. It must have very low offset and high DC gain.

5.2.1 Low offset

Equation (14) shows the largest possible signal at the amplifier's input is inversely proportional to its gain and proportional to the amplifier's output. It is also true the output cannot exceed its linear operation-region. So the absolute value of the offset in the

comparator must be much smaller than the input signal so the polarity in the amplifier can be measured.

5.2.2 High gain

Because the total output conductance increases with the output swing, the output level should be limited to certain value so near-operating-point DC gain can be measured accurately. Assuming the amplifier's output is 10 times less than the 'digital high', the comparator must have 10 times more gain than the amplifier so a correct digital level signal can be generated. Because the DC-gain of the amplifier is targeted to be very high, it is necessary to design a comparator with a much higher gain in order to amplifier input correctly. Meanwhile, the comparator's offset should be very low. This becomes a very difficult task and significantly limits the performance of the amplifier.

5.3 Real test setup

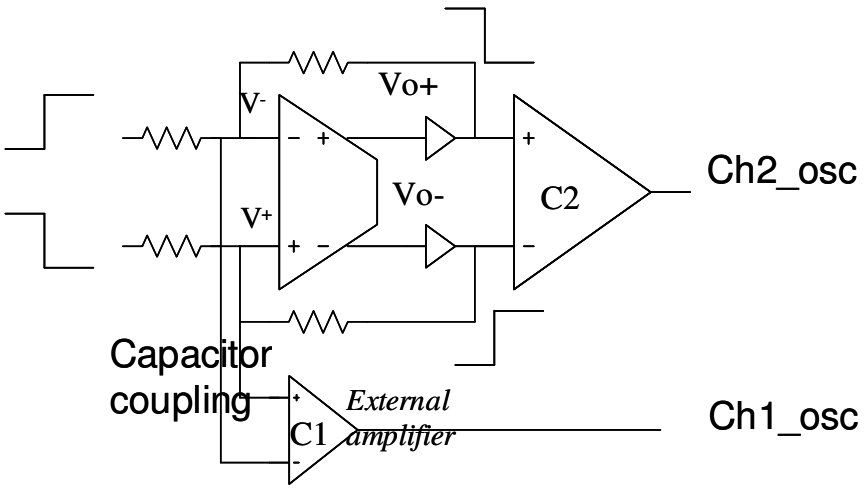
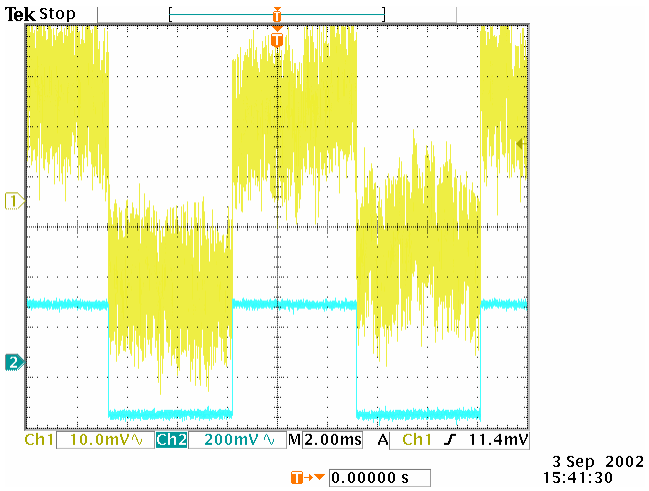


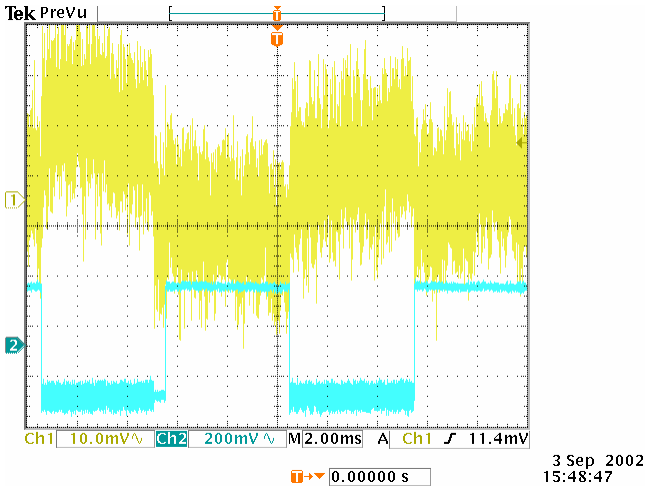
Fig. 14 test setup

Because of these difficulties, the automatic measurement was not implemented. Instead, AC-coupling and an external amplifier were used while measuring phase with an oscilloscope. Fig. 14 shows the final setup in testing.

5.4 Measurement



a)



b)

Fig. 15 captured waveforms with a) in-phase; b) phase-inversion

MOSIS delivered 5 chips with package. Manual tuning was based on phase-inversion detection. Fig. 15 shows captured waveforms with both in-phase and phase-inversion cases.

All 5 chips were tested and measurement is summarized in Table 2-1. The minimal DC gain at room temperature is 84.5dB while the maximum gain exceeded 90dB even though it could not be measured accurately.

Table 2-1 Measured DC gain of fabricated chips

Chip	#1	#2	#3	#4	#5
Gain(dB)	90	87.6	89.3	84.5	86.5

Output-level dependent gain was also observed. Using different control-code at different output level, the dropped-DC gain was re-enhanced, and >76dB DC gain over 2Vpp was maintained. Measurement results were compared to simulation results, and both matched quite well as shown in Fig. 16.

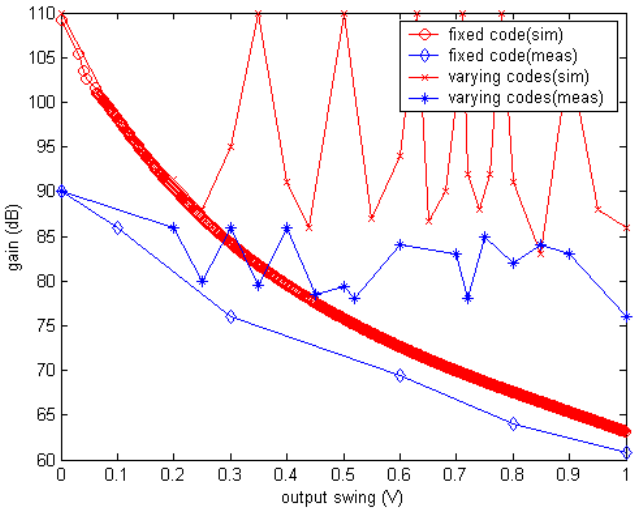


Fig. 16 measured and simulated amplifier's DC gain

VI. Conclusions

A single-stage, full-differential, positive-feedback amplifier with more than 80dB gain over wide output swing in standard digital CMOS was designed. It stacks only 3 transistors from supply to ground, which makes it low-voltage applicable with excellent frequency response thanks to the single-stage structure. A modified testing method using digital-level testing result based on phase-inversion detection was proposed. Unlike most positive-feedback amplifier structures, which are highly reliant on fabrication matching and whose gain drops quickly with output swing, the proposed amplifier uses a newly invented, digital-programmable precision MOS attenuator, an output-level monitor circuit block, and a specific tuning and mapping scheme to maintain its high gain over the whole output swing. With the integration of a sufficient resolution- and range-programmable DAC attenuator, this amplifier can achieve high gain over process, supply, and temperature variations, which improves fabrication yield dramatically without significantly increasing cost.

This single-stage positive feedback is well suited to drive capacitive load and a capacitive feedback network. It can be used in high-speed, high-resolution data converters, high-speed comparators, and can also function as a basic analog building block in large systems. It will significantly reduce fabrication costs for mixed-signal systems in low-voltage applications.

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CHAPTER 3. AUTOMATIC TUNING OF POSITIVE FEEDBACK AMPLIFIERS USING DIGITAL POST PROCESSING TECHNIQUES BASED ON DYNAMICAL SYSTEMS AND BIFURCATION THEORY

A paper accepted by IEEE Transactions on circuits and systems I

Chengming He, Le Jin, Degang Chen, Randall Geiger

Abstract: A positive feedback differential CMOS amplifier (PFA) and inherent nonlinearity in its DC transfer curve were analyzed. Based on nonlinear dynamic systems and bifurcation theory, we predicted bifurcation and hysteresis phenomena in the PFA. An algorithm, which can be implemented using simple digital logic, was developed to measure the PFA's open-loop stability as the bifurcation parameter changes. Parameter-tuning algorithms were constructed that systematically move the amplifier's operational point towards the bifurcation point, at which infinite DC gain happens. In order to compensate for the PFA's high sensitivity to process and temperature variations, flexible analog design integrating digital programmability and inexpensive and adaptive digital post-processing techniques were developed. This flexibility and post-processing capability could dramatically enhance the PFA's yield. Full corner simulation results over wide temperature range verified the bifurcation phenomena and the effectiveness of the control algorithms. It is shown that this amplifier can maintain high performance in the most advanced digital CMOS technology at very low voltage supply. They also demonstrate that the proposed approach offers a robust PFA design with both high yield and high performance.

Key words: high gain, amplifier, and bifurcation

I. Introduction

Recently, experts identified System-on-a-chip (SOC) as one of the next generation drivers for the semiconductor industry [1]. Integrating analog functions in SOC is the trend and low cost is a key to success. In particular, high performance mixed-signal SOCs in inexpensive standard digital CMOS processes will be in high demand. However, the same group of experts also identified mixed-signal design as a difficult challenge and analog circuit design as a bottleneck in the process towards SOC.

The operational amplifier, or Op-amp, is by far the most common and important category analog circuit. Because of the success of MOS technologies, the MOS Op-amp design has become one of the most important analog circuit designs. Realization of high performance MOS amplifiers in standard digital CMOS is a key to implementing low-cost mixed-signal SOCs. Among these MOS amplifiers, high gain high speed amplifier is one especially important category.

Cascoding with gain-boosting and multi-stage cascading have been proven to be effective in achieving high gain with moderate-to-high voltage supplies. On the other hand, positive-feedback technique has been shown to be more promising in achieving high DC gain with good frequency response in low-voltage applications [9-13]. A pre-amplifier with positive feedback is often used for high-speed comparators. The pre-amplifier uses cross-coupled and diode-connected MOSFET pairs. Transconductance g_m of the cross-coupled pair acts as negative conductance and g_m of the diode-connected pair acts as positive conductance. This structure will have hysteresis when the negative conductance is larger than the positive

one. However, high-gain amplifier design prefers no-hysteresis as well as good matching between the positive and negative conductance. It is challenging to achieve high yield due to the difficulty of matching as well as the temperature and process variations. Previous studies concluded that achieving a fixed positive feedback amplifier design under all variations would gain little improvement while adding too much cost. Yan [12] introduced a continuous-time adjusting scheme to digitally calibrate the positive feedback amplifier. He [13] investigated a discrete adjusting scheme to calibrate the positive feedback amplifier. Both [12] and [13] used phase-inversion-detection techniques and enhanced amplifier's gain and yield. However, they required high-gain low-offset comparators which are difficult to realize and required heavy human-interferences, making calibration time-consuming and amplifiers expensive. Low yield as well as high cost is still the major limitations.

Furthermore, such positive-feedback amplifiers show strong non-linearity [12, 13]. Efforts have been made to decrease the gain dependence on output swing but few achieved a practical solution. Traditional circuit designers typically use linear models [14] to study analog circuits or even call those circuits "linear circuits", but nonlinearity in circuits becomes more apparent with feature size shrinking. Although linear models are still valid in certain applications, knowing the non-linearity in circuit/device level can help us identify circuit non-ideality, avoid the disadvantages of non-linearity and even make use of the advantages of nonlinearity.

This work resolves the main limitation of yield in the PFA by introducing adaptive-feedback control based on the discovery of bifurcation. The work also enhances understanding of circuit performance with the help of the nonlinear dynamic systems theory. This paper first introduces bifurcation phenomenon in non-linear dynamic systems [15].

Section III provides theoretical analysis of dynamic behavior in a positive feedback amplifier [13]. This analysis also explains the nonlinearity in the positive feedback amplifier. Parameter dependency of bifurcation [15] is used to study the positive feedback amplifier, and bi-state detection with pull-up and pull-down is developed to maintain a high DC gain. Section IV discusses two digital post-processing techniques, bifurcation detection and branching parameter driving algorithms. Both algorithms were verified valid using MATLAB™ as well as Cadence™ mixed-signal simulation tools. These algorithms do not require high-gain low-offset comparators, which overcome the shortcoming of [12] and [13]. Section V presents system and circuit level simulation results using industrial BSIM3v3 models and section VI concludes this paper.

II. Dynamical Systems and Bifurcation Theory

Bifurcation [15] is one commonly encountered nonlinear phenomenon in dynamical systems. In order to explain bifurcation clearly, differential equation (1) is introduced,

$$\dot{y} = (\mu - \mu_0)\, y - y^3, \tag{1}$$

where μ_0 is a constant. For $\mu > \mu_0$, there are two stable equilibria, $y = \pm\sqrt{\mu - \mu_0}$ and one unstable equilibrium $y_0 = 0$. For $\mu \le \mu_0$, there is only one stable equilibrium at $y_0 = 0$. We call point ($y_0 = 0$, μ_0) a *bifurcation point* and μ the *branching parameter*. Fig. 1 shows the *branch diagram* of this supercritical pitchfork bifurcation.

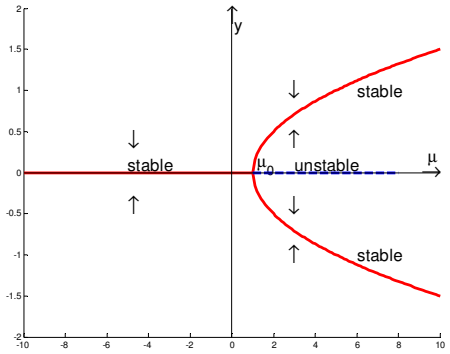


Fig. 1 supercritical pitchfork bifurcation

Bifurcation points can be identified through certain algebraic properties. Let

$$f(y,\mu) = (\mu - \mu_0)y - y^3 . \tag{2}$$

We can get the derivatives of $f(y,\mu)$ respect to y and μ as

$$f_y(y,\mu) = (\mu - \mu_0) - 3y^2 ,$$

and

$$f_\mu(y,\mu) = y . \tag{3}$$

If the matrix $[\, f_y(y_0,\mu_0)\ f_\mu(y_0,\mu_0)\,]$ is singular, the point (y_0,μ_0) is a bifurcation point.

In the supercritical pitchfork case, $[\, f_y(y_0,\mu_0)\ f_\mu(y_0,\mu_0)\,]$=[0 0]. This suggests the branching point (y_0,μ_0) is a bifurcation point.

It can be shown that y will converge to $y_0 = 0$ with time going when $\mu \le \mu_0$ no matter how the initial condition is. If $\mu > \mu_0$, y will converge to $y = \sqrt{\mu - \mu_0}$ when $y\big|_{t=0} > 0$ or converge to $y = -\sqrt{\mu - \mu_0}$ when $y\big|_{t=0} < 0$ (shown in Fig. 1). Thus, it is possible to detect and move the branching parameter μ to μ_0. In the following sections, we will demonstrate the application of bifurcation in the realization of a high performance analog function.

III. Positive Feedback Amplifier

Fig. 2 depicts a positive feedback amplifier [13], where the gates of PMOS transistors (current source load) are connected to its output through a feedback buffer with attenuation of μ. Using small signal equivalence shown in Fig. 3 to analyze the positive feedback amplifier, we can show the amplifier has an attenuation-dependent DC gain (4),

$$A = \frac{g_{mn}}{g_{op} + g_{on} - \mu g_{mp}}, \tag{4}$$

where $g_{op} = \lambda_p \beta_p V_{EBP}^2$, $g_{on} = \lambda_n \beta_n V_{EBN}^2$, $g_{mn} = 2\beta_n V_{EBN}[1 + \lambda_n (V_{OCM} - V_{SS})]$, and $g_{mp} = 2\beta_p V_{EBP}[1 + \lambda_p (V_{DD} - V_{OCM})]$. Define

$$\mu_0 = \frac{g_{op} + g_{on}}{g_{mp}}, \tag{5}$$

we can see that the amplifier will have an infinite DC gain when $\mu = \mu_0$.

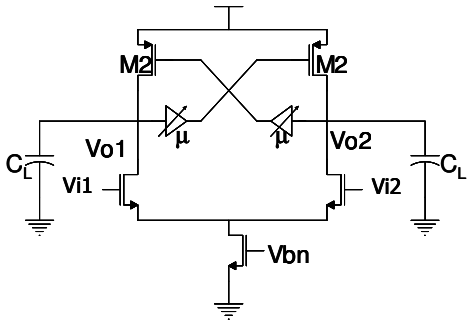


Fig. 2 a positive feedback amplifier

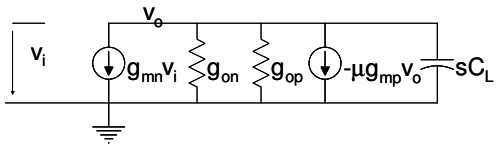


Fig. 3 small signal equivalence of the positive feedback amplifier

However, we need more information to search and maintain the optimal attenuation over process and temperature variations, where the nonlinear dynamic theory is found to be helpful [16].

A. Amplifier's dynamic

Level 1 Schichman-Hodges model [17] is used to derive the system dynamic. This model includes the channel length modulation effect where $I = \beta V_{EB}^2 (1 + \lambda |V_{DS}|)$. We denote $V_{EBN} = V_{GSN} - V_{THN}$, $V_{EBP} = V_{SGP} + V_{THP}$, $V_{i1} = V_{ICM} + v_{i1}$, $V_{i2} = V_{ICM} + v_{i2}$, $V_{o1} = V_{OCM} + v_{o1}$, and $V_{o2} = V_{OCM} + v_{o2}$. Using these denotations, the dynamic of this amplifier can be written as

$$C_L \frac{dv_{o1}}{dt} = \beta_p (V_{EBP} - \mu v_{o2})^2 [1 + \lambda_p (V_{DD} - V_{OCM} - v_{o1})] - \beta_n (V_{EBN} + v_{i1})^2 [1 + \lambda_n (V_{OCM} + v_{o1} - V_S)]$$

$$C_L \frac{dv_{o2}}{dt} = \beta_p (V_{EBP} - \mu v_{o1})^2 [1 + \lambda_p (V_{DD} - V_{OCM} - v_{o2})] - \beta_n (V_{EBN} + v_{i1})^2 [1 + \lambda_n (V_{OCM} + v_{o2} - V_S)]. \quad (6)$$

For simplicity, we will use $v_{i1} = -v_{i2} = v_i / 2$ and $v_o = v_{o1} - v_{o2}$ in our later discussions. If the circuit has very good common mode reject ratio (CMRR), we have $v_{o1} = -v_{o2} = \frac{v_o}{2}$. By letting $y = v_o$, $x = v_i$, (6) can be rewritten as

$$\dot{y} = -\frac{g_{op} + g_{on} - \mu g_{mp}}{C_L} y - \frac{\mu^2 \beta_p \lambda_p}{4C_L} y^3 - \frac{\beta_n \lambda_n [1 + \lambda_n (V_{OCM} - V_S)] x^2}{4C_L} y - \frac{g_{mn}}{C_L} x. \quad (7)$$

B. DC transfer characteristics

In equation (7), solving $\dot{y} = 0$ gives us the amplifier's DC transfer characteristics,

$$\mu^2 y^3 + [a(\mu_0 - \mu) + bx^2] y + cx = 0, \quad (8)$$

where $a = 4 g_{mp} / \beta_p / \lambda_p$, $b = \beta_n \lambda_n [1 + \lambda_n (V_{OCM} - V_S)] / \beta_p / \lambda_p$ and $c = 4 g_{mn} / \beta_p / \lambda_p$.

Fig. 4 shows the solution to (8). When $\mu \leq \mu_0$, the DC transfer curve of the positive feedback amplifier behaves like an open-loop amplifier. However, when $\mu > \mu_0$, the circuit shows hysteresis in its DC transfer curves. It is really interesting to study this unusual property.

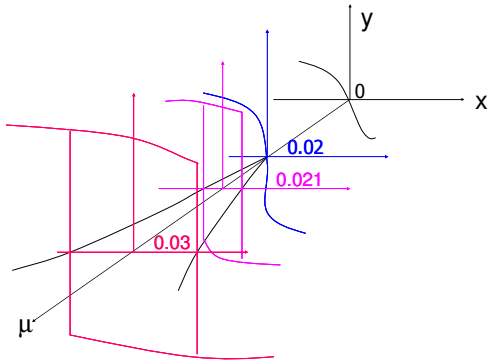


Fig. 4 DC transfer curves of the positive feedback amplifier.

C. Bifurcation without excitation

When x=0, we rewrite (8) as

$$\mu^2 y^3 + a(\mu_0 - \mu) y = 0. \tag{9}$$

It turns out that for $\mu > \mu_0$ there are two stable equilibria with $y = \pm\sqrt{a(\mu - \mu_0)/\mu^2}$ and one unstable equilibrium $y_0 = 0$, whereas for $\mu \leq \mu_0$ there is only one stable equilibrium $y_0 = 0$. Fig. 5 shows the branching diagram. The symmetry of the branching diagram with respect to the μ-axis reflects the basic assumption of perfect symmetry.

This branching diagram has a branching point at

$$(y_0, \mu_0) = (0, (g_{op} + g_{on})/g_{mp}). \tag{10}$$

It is easy to show that $[\, f_y(y_0,\mu_0)\ \ f_u(y_0,\mu_0)\,]=[0\ \ 0]$. Thus, the branching point $(y_0,\mu_0)=(0,(g_{op}+g_{on})/g_{mp})$ is a bifurcation point. Due to limited supply voltage in real circuits, amplifier's outputs saturate when the branching parameter is large enough, as shown in Fig. 5.

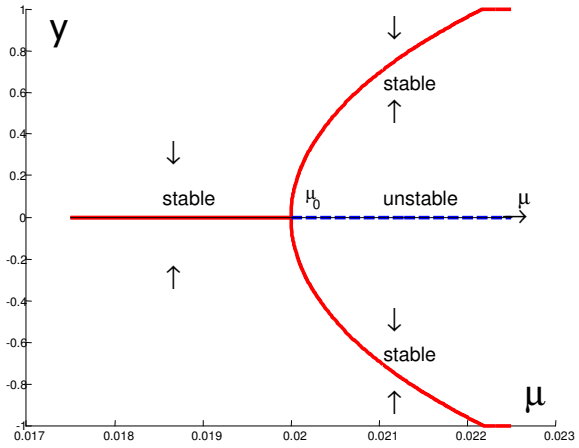


Fig. 5 branching diagram when x=0

D. Bifurcation with excitation

When x≠0 and x is small, the branching diagram in *y*-μ plane shows discontinuity for the two branches of stable equilibriums. Solution of the equation (8) suggests there exists a one-one mapping between y and x that when $\mu < \mu_0 + \frac{bx^2}{a}$, as shown in Fig. 6.

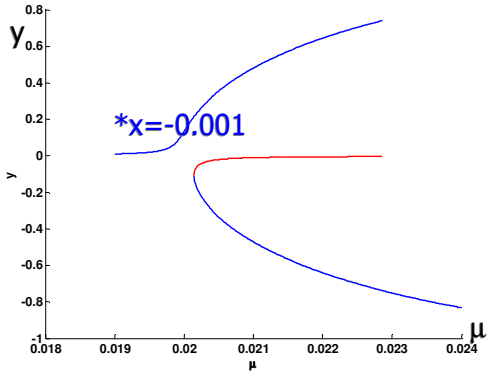


Fig. 6 bifurcation with non-zero excitation

The solution for $f(y,x,\mu)=0$ becomes complex when $\mu \geq \mu_0 + \frac{bx^2}{a}$. One-One mapping from x to y turns to be invalid. When $|x| < x_0$, we can find two stable equilibria points and an unstable equilibrium. When $|x| > x_0$, there will be only one stable equilibrium point. x_0 is given by a solution to equation (7) and (11)

$$\frac{\partial f(y,x,\mu)}{\partial y} = -\frac{g_{op}+g_{on}-\mu g_{mp}}{C_L} - \frac{3\mu^2\beta_p\lambda_p}{4C_L}y^2 - \frac{\beta_n\lambda_n[1+\lambda_n(V_{OCM}-V_S)]x^2}{4C_L} = 0. \qquad (11)$$

One will get equation (12) combining equation (7) and (11)

$$(g_{op}+g_{on}-\mu g_{mp}) + \frac{3\mu^2\beta_p\lambda_p}{4}\left(\frac{2x}{\mu^2\beta_p\lambda_p}\right)^{2/3} + \frac{\beta_n\lambda_n[1+\lambda_n(V_{OCM}-V_S)]x^2}{4} = 0. \qquad (12)$$

Solution of (12) suggests that in order to observe bifurcation, one has to limit excitation to be a small value, especially when the branching parameter is close to the bifurcation point.

Fig. 4, 5 and 6 all suggest bi-state stability presents in this non-linear system when branching parameter $\mu > \mu_o$.This bi-state stability will lead to hysteresis in the amplifier's

DC transfer characteristic. This hysteresis in this supercritical pitchfork bifurcation provides a way to detect if branching parameter μ is larger than the bifurcation point or not.

E. DC gain and its nonlinearity

Based on the definition used in circuit design area, DC gain at operating point (0,0) (either stable or unstable) is the tangent of $f(y,x,\mu)$ at $(0,0,\mu)$ in (y,x) plane, shown in equation (13)

$$A\big|_{(0,0,\mu)} = \frac{f_x(0,0,\mu)}{f_y(0,0,\mu)} = -\frac{g_{mn}}{g_{op}+g_{on}-\mu g_{mp}}. \tag{13}$$

Let $\mu_0 = \frac{g_{op}+g_{on}}{g_{mp}}$, this suggests that at bifurcation point $(0,0,\mu_0)$, the positive feedback amplifier will achieve an infinite DC gain. μ_0 is typically smaller than 1. Fig. 7 illustrates the DC transfer characteristic of the amplifier at bifurcation point.

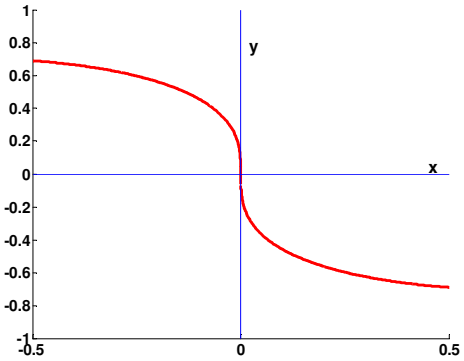


Fig. 7 branching diagram with respect to input at bifurcation point ($\mu = \mu_0$)

The DC transfer curve in Fig. 7 shows large nonlinearity. From equation (7), we can derive the small signal gain (the tangent slope of this DC transfer curve) as

$$A\big|_{(y,x,\mu)} = \frac{f_x(y,x,\mu)}{f_y(y,x,\mu)} \approx -\frac{g_{mn} + \frac{\beta_n \lambda_n xy}{2}}{g_{on} + g_{op} - \mu g_{mp} + \frac{3\mu^2 \beta_p \lambda_p y^2}{4} + \frac{\beta_n \lambda_n x^2}{4}}. \tag{14}$$

This analysis is valid for any μ value. At the operating range, $g_m >> \frac{\beta_n \lambda_n xy}{2}$, $g_o >> \beta\lambda(x^2 + y^2)$, $y^2 \geq x^2$.When $\mu = 0$,

$$A\big|_{(y,x,0)} = -\frac{g_{mn} + \frac{\beta_n \lambda_n xy}{2}}{g_{on} + g_{op} + \frac{\beta_n \lambda_n x^2}{4}}. \tag{15}$$

For a traditional amplifier, $y^2 \geq x^2$, the numerator will dominate the amplifier's gain nonlinearity. This nonlinearity will limit the performance of certain ADCs using open-loop amplifier approach. For an ideal positive feedback amplifier, $\mu = \mu_0$,

$$A\big|_{(y,x,\mu)} \approx -\frac{g_{mn} + \frac{\beta_n \lambda_n xy}{2}}{\frac{3\mu^2 \beta_p \lambda_p y^2}{4} + \frac{\beta_n \lambda_n x^2}{4}}. \tag{16}$$

Equation (16) shows the denominator determines the gain nonlinearity of a positive feedback amplifier and suggests that DC gain rolls off in a rate proportional to the output swing square. This explains why the positive feedback amplifier shows so strong open-loop nonlinearity, which was shown in [12] as a bell-shape curve.

Equation (16) also suggests that reducing λ will significantly increase open loop gain at non-zero outputs given the factor that output conductance of a MOS transistor is proportional to channel-length modulation factor λ. Equation (17) gives the detail analysis.

$$\mu = \frac{g_{op} + g_{on}}{g_{mp}} \propto \lambda ,$$

$$A \propto \frac{1}{\lambda x^2 + C\lambda^3 y^2} . \tag{17}$$

The authors [18] showed a relationship between open-loop gain and close-loop gain linearity. For a positive feedback amplifier with an infinite DC gain at operating point, the gain linearity of a close-loop configuration can be written as (18)

$$THD \geq 20\log(\left|\frac{y_m}{x_m}\right|), \tag{18}$$

where y_m is the desired output swing, x_m is the input value given a specific DC transfer curve. Equation 17) implies that given y_m fixed, decreasing λ will reduce x_m dramatically. Thus, decreasing λ enhances the gain linearity of a close-loop configuration using the positive feedback amplifier. Increasing L is the most effective way to decrease λ. However, this will slow down the transistor's speed. Thus one should take a tradeoff between gain and speed for different specifications.

F. Effect of offset on bifurcation

All the above analyses assume perfect symmetric matching. However, semiconductor fabrication steps will introduce random variation and mismatch from devices to devices, from die to die, from wafer to wafer and from lot to lot; imperfect layout will cause deterministic mismatch, for example, non common-centroid pattern will introduce linear gradient mismatch. In this work, input-referred offset is used to model the asymmetric property. Good layout can help to reduce or even eliminate deterministic offset but it can

never remove random offset. After an amplifier has been fabricated and packaged, offset for this amplifier is fixed.

Assume an amplifier has offset V_{OS}, actual excitation seen by the amplifier is $x = x_e + V_{OS}$ when an external excitation x_e is applied on the amplifier. Thus, the differential equation (7) should be modified as

$$\dot{y} = -\frac{g_{ot}}{C_L} y - \frac{\mu^2 \beta_p \lambda_p}{4C_L} y^3 - \frac{\beta_n \lambda_n [1 + \lambda_n (V_{OCM} - V_S)](x_e + V_{OS})^2}{4C_L} y - \frac{g_{mn}}{C_L}(x_e + V_{OS}), \quad (19)$$

where $g_{ot} = g_{on} + g_{op} - \mu g_{mp}$.

Equation (19) implies that bifurcation will still happen. The only difference is that the whole DC transfer curve will center at the offset voltage instead of the origin.

G. Possible gain enhancement

Early discussion has shown that the positive feedback amplifier will achieve an infinite DC gain at the bifurcation point. So keeping the amplifier at bifurcation point becomes the most important task. However, the positive feedback amplifier is high sensitive to process and temperature variations. Previous studies have concluded that a fixed-design of the positive feedback amplifier could only gain very little while adding too much more cost. Early discussions suggest that we can move the branching-parameter μ to change bifurcation. A fixed design cannot provide such capability of change. Thus we designed a variables precise CMOS attenuator [13] to provide sufficient coverage of the branch parameter, shown in Fig. 8, and developed specific algorithms to find the bifurcation point.

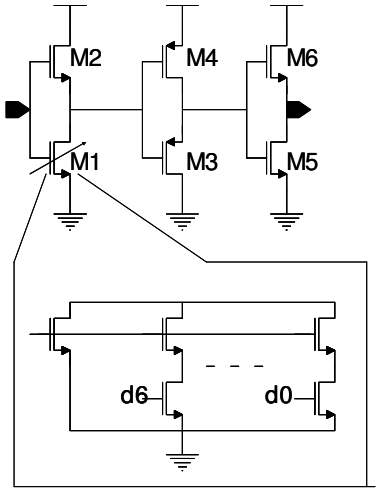


Fig. 8 a digital programmable precise CMOS attenuator

These control algorithms utilize digital post-processing techniques which could be implemented either in programmable micro-controller or hard-wired with application-specific integrated circuit (ASIC), both in digital CMOS processes. This approach saves cost and favors more advanced deep sub-micro CMOS processes.

Instead of adjusting branching parameter continuously, digital controlled discrete branching parameter searching is used. As shown in Fig. 8, this digital programmable precise CMOS attenuator consists of three-stage linear MOS attenuators [20] which provide necessary quiescent-voltage shift and decreases sensitivity to single transistor size variation as well as having a minimal step of Δ. The first stage linear MOS attenuator has 7-bit control (Γ) so the total attenuation (nominal) can be expressed as

$$\mu = \mu_{\min} + \Delta\Gamma . \tag{20}$$

Design of the discrete step attenuator and bifurcation-tuning guarantees a minimal DC gain at operating point expressed in (21)

$$\left|A_{\min}\right| = \frac{g_{mn}}{g_{on} + g_{op} - \mu_{opt} g_{mp}} \geq \frac{g_{mn}}{\Delta g_{mp}} . \tag{21}$$

The positive feedback amplifier achieves a very high DC gain by selecting an optimal control code to eliminate the bifurcation. At this condition, we have $\mu < \mu_0$ and $0 < g_{res} = g_{on} + g_{op} - \mu_{opt} g_{mp} < \Delta \cdot g_{mp}$. Because of process variations, g_{res} becomes a random variable. Without loss of generality, we assume g_{res} follows a uniform distribution between 0 and $\Delta \cdot g_{mp}$. With this assumption, we will find that the average gain enhancement using bifurcation approach becomes ∞ [19]. Although the random variable g_{res} may not follow the assumption of uniform distribution, average gain enhancement of the positive feedback amplifier using our proposed bifurcation-tuning will be sufficient large.

H. Performance summary with $\mu = \mu_0$

Table 3-1 Summary for the positive feedback amplifier at bifurcation point

	Fig. 2
Tail current	I
Average DC Gain	∞
Gain-Bandwidth Product	g_{mn} / C_L
Phase Margin	90°

Table 3-1 lists the performance summary for the amplifier shown in Fig. 2. Without scarifying power efficiency on gain-bandwidth, our proposed amplifier achieved infinite DC gain enhancement on average, assuming the proposed searching procedure generates uniformly distributed residual conductance.

IV. Bifurcation Detection and Parameter Tuning Algorithms

The above analyses suggest that it is possible to design high performance analog amplifiers using bifurcation. However, it is important to know how to properly set the branching parameter to be very close to the bifurcation point and, if it is not there, how to drive it back. We will construct robust methods to detect bifurcation. Based on the bifurcation, we will develop fast and robust algorithms to drive branching parameter μ back to the bifurcation point.

A. Bi-state detection with pull-up/down and bifurcation detection algorithm

Previous analyses suggest two stable equilibria exist when $\mu > \mu_0$ and $x = 0$ or within very small input range. When the output stays at either stable equilibrium, disturbance will not change the output state. Fig. 9 illustrates this DC transfer with $\mu > \mu_0$.

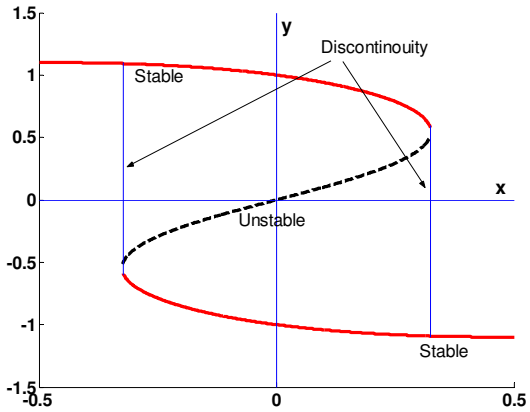


Fig. 9 DC transfer of the positive feedback amplifier with large μ

This leads to a bi-state detection circuit by shorting input and setting initial conditions with pull-up/pull-down circuits, as shown in Fig. 10. It consists of the core amplifier, an extra

low gain comparator (C1) and two pairs of switches. The amplifier's output will be set to either high or low by pulling up to the positive supply or down to the ground.

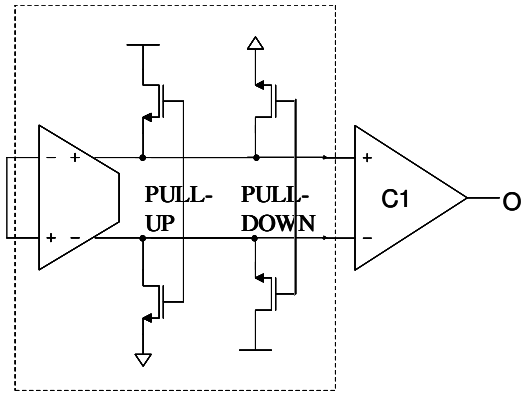


Fig. 10 bi-state detection with pull-up/pull-down circuits

Depending on the bifurcation parameter, the output may finally settle to the same value or settle to two different values. If the comparator gives the same results after the pull-up and pull-down operations, non-bifurcation is determined. On the contrary, if the comparator gives different answers from pull-up to pull-down operation, bifurcation is detected. These procedures are used to develop the bifurcation detection algorithm called **Bifurcation_detect**(μ), as shown in Fig. 11. This algorithm works well for supercritical pitchfork bifurcations.

Assuming $\mu > \mu_0$, the positive feedback amplifier will stay at one of these two stable equilibria $y = \pm\sqrt{\frac{4(\mu g_{mp} - g_{op} + g_{on})}{\mu^2 \beta_p \lambda_p}}$, which is insensitive to noise. As shown in Fig. 4 and 5, these two equilibria become large even when μ is a little away from μ_0. One can use a low gain comparator to digitalize it easily (O_H *and* O_L). We will expect $O_H \neq O_L$ when $\mu > \mu_0$ while $O_H = O_L$ when $\mu \leq \mu_0$ confidently.

Step 0: Make excitation to be 0 (short differential inputs).

Step 1: pull-up output y to be high (e.g., y=1)

Step 2: release y and wait y to be stable

Step 3: >0 decision O_H

Step 4: pull-down output y to be low (e.g. y=-1)

Step 5: release y, wait y to be stable

Step 6: >0 decision O_L

Step 7: compare O_H *and* O_L

If $O_H = O_L$ *return no*

else return yes

End

Fig. 11 a bifurcation detection algorithm

B. Branching parameter tuning algorithms

Assuming $\mu_L < \mu_o, \mu_H > \mu_o$, one cannot observe bifurcation when $\mu \in [\mu_L, \mu_o]$ and one may observe bifurcation when $\mu \in (\mu_0, \mu_H]$. Due to this bi-state monotonic property, we can use a linear searching algorithm or a bisection-searching algorithm to drive branching parameter μ.

B.1 Linear searching algorithm

Assume $[\mu_L, \mu_H]$ is divided into k ($k \in N$) equal distance sections $\Delta = \frac{\mu_H - \mu_L}{k}$

Mathematically one can adjust μ continuously when $k \to \infty$. After the searching is done, the amplifier will be in non-bifurcation mode while the branching parameter is in 1LSB

range of the ideal bifurcation point μ_o .Fig. 12 and Fig. 13 show two possible linear searching algorithms.

Start: Initial $\mu = \mu_L$

Loop A: bifurcation_detect(u)

If (no)

$\mu := \mu + \Delta$

Goto A;

Else

$\mu := \mu - \Delta$

Goto B;

B: end

Fig. 12 a linear bifurcation parameter searching algorithm from μ_L

Start: Initial $\mu = \mu_H$

Loop A: bifurcation_detect(μ*)*

If (yes)

$\mu := \mu - \Delta$

Goto A;

Else

Goto B;

B: end

Fig. 13 a linear bifurcation parameter searching algorithm from μ_H

B.2 A bisection-searching algorithm

Fig. 14 shows this algorithm search μ_o within $[\mu_L, \mu_H]$

Start: Initial $\mu = \frac{\mu_H + \mu_L}{2}$

Loop A: bifurcation_detect(μ)

If yes

$\mu_H := \mu$;

$\mu := \frac{\mu_H + \mu_L}{2}$

If($\mu_H - \mu_L \le \varepsilon$)

$\mu := \mu_L$;

Goto B;

Else

Goto A;

Else

$\mu_L := \mu$;

$\mu := \frac{\mu_H + \mu_L}{2}$;

If($\mu_H - \mu_L \le \varepsilon$)

$\mu := \mu_L$;

Goto B

Else

Goto A

B: end

Fig. 14 bisection bifurcation parameter searching algorithm

All these algorithms use the conceptual circuit illustrated in Fig. 15.

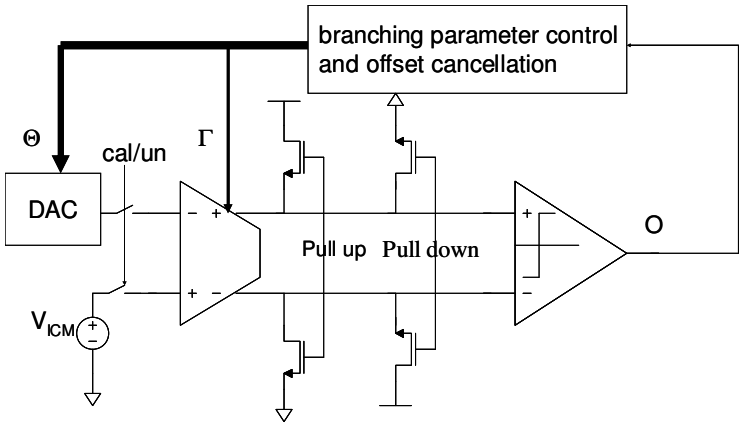


Fig. 15 automatic branching parameter searching circuit

Because a small offset in the amplifier will saturate the output, all these algorithms require offset compensation. One high resolution DAC is needed to cancel offset effects.

C. Improved branching parameter searching algorithm

Conceptually offset should be pre-compensated before trying to execute the bifurcation detection procedure. However, it is not so practical to judge offset in an open-loop high-gain amplifier. Thus it is nearly impossible to do offset cancellation separately. Fortunately, bifurcation detection has the potential to tell both input information and bifurcation status information.

As shown in Fig. 16, the amplifier input range is divided into three regions:

A: smaller than the lower boundary of bifurcation B_L;

B: bifurcation region (B_L, B_H);

C: larger than the upper boundary of bifurcation B_H.

$B_L < B_H$ when the bifurcation parameter $\mu > \mu_0$ and $B_L = B_H$ when $\mu \le \mu_0$. Denote $L = B_H - B_L$.

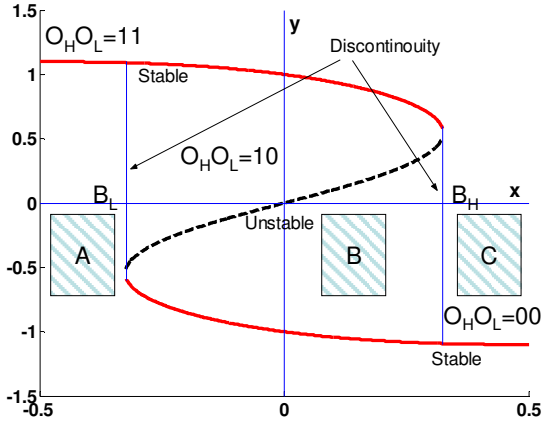
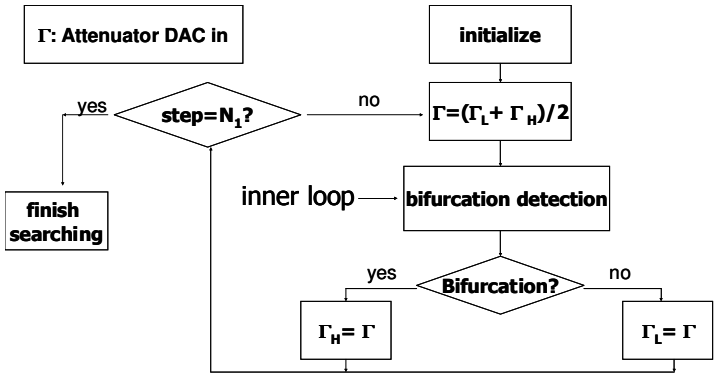


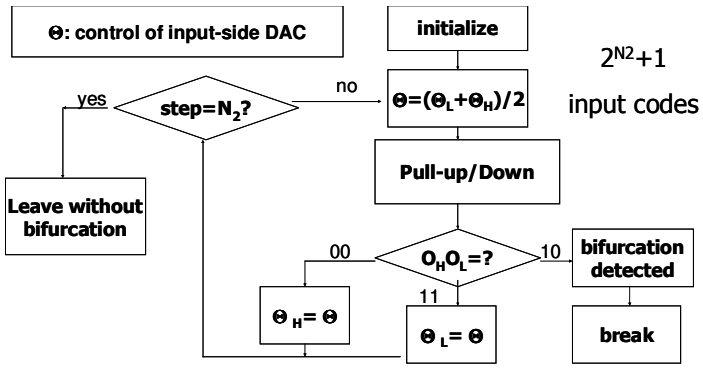
Fig. 16 different results with pull-up/pull-down operations

Both pull-up and pull-down operations will stay high in region A while stay low in region C. In region B, pull-up operation will stay high while pull-down operation will stay low. Offset is automatically considered by this type of operations. Thus we can devise this pull-up and pull-down operation and use their outputs to adaptively adjust input signal. Input signal will be increased if both are high while it is reduced when both are low. When the two outputs are different, bifurcation has been detected thus input signal has been in the bifurcation window and this fulfills the major function of these operations.

Based on these observations, a two-loop bifurcation-point searching algorithm was proposed—the inner loop of sweeping input and detecting bifurcation while the outer loop tuning bifurcation parameter μ. This algorithm is shown in Fig. 17. In our design, the attenuator is a N1-bit (7-bit) DAC (Fig. 8) and the input DAC is a N2-Bit (16-bit) pre-distortion R-2R DAC. Without complicating analysis, both DAC are considered to be positive slope with respect to their control codes.



a)



b)

Fig. 17 a) bifurcation-parameter pushing algorithm; b) bifurcation-detecting algorithm

D. Property of input-side DAC and attenuator DAC

In order to compensate all possible offset, the DAC should have sufficient coverage. Furthermore, all tiny bifurcation windows should be trigged in order to catch possible bifurcation with the optimal attenuation factor, it is preferred that all tiny bifurcation windows can be triggered in. Simulations show that input of 10uV with 80dB unstable gain may cause 0.01V hysteresis output. This 10uV hysteresis input was considered to be detectable range L_{spec}. Thus a high resolution DAC with analog out $\chi(\Theta)$ from a digital

code Θ is needed. These lead to two main design constraints—sufficient coverage of offset and small positive jump in DAC output change, as equation (22) and (23)

$$\chi(\Theta = 0) < Offset_{\min} < Offset_{\max} < \chi(\Theta = 2^{N2}) \tag{22}$$

$$\varepsilon_{\chi} = \max_{0 \le \Theta \le 2^{N2}-1} \{\chi(\Theta + 1) - \chi(\Theta)\} \le L_{spec} \tag{23}$$

It turns to be very tedious to get accurate boundary of offset and necessary resolution, specifications are based on some experiments and empirical knowledge with sufficient margin. That's why a 16-bit DAC with 0.2V full range was proposed.

Input-side 16-bit DAC sounds a very expensive, area-consuming and difficult design. In reality, it is really a lousy DAC with a small positive step and possible large negative jump R-2R DAC. This R-2R ladder has been pre-distorted to be R-1.8R so that no large positive jump exists. Fig. 19 shows the 8-bit MSB in the 16-bit DAC transfer. Simulated largest positive jump is only 5uV while negative jump can go to 0.01V.

Fig. 18 shows the 16-bit DAC transfer curve (8-bit MSB is used to illustrate the transfer.). Simulated largest positive jump is only 5uV while negative jump can go to 0.01V.

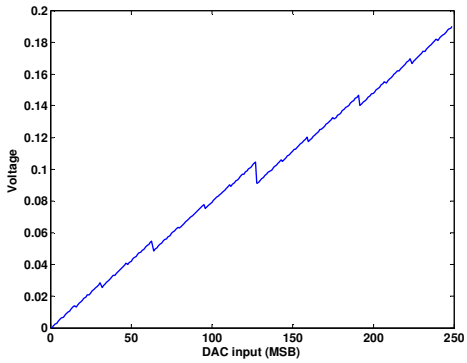


Fig. 18 offset compensation DAC characteristic (only 8-MSB was shown)

A 7-bit monotone attenuator DAC was designed to cover desired attenuation range over PVT variations. Fig. 19 shows its transfer characteristics.

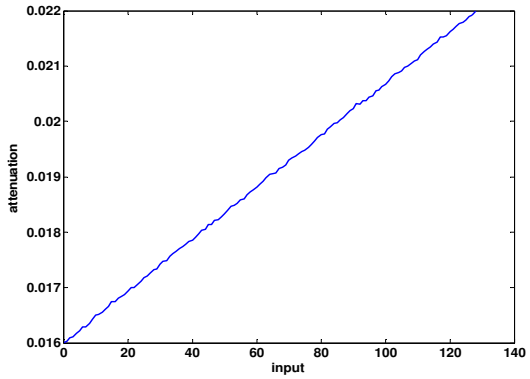


Fig. 19 attenuator DAC linearity

E. Implementation of the two-loop binary searching algorithm

The proposed two-loop optimal bifurcation parameter tuning algorithm can be realized in integrated-circuits using finite-state-machine (FSM) approach. The flowchart shown in Fig. 17 clearly expressed necessary state-flow. This algorithm is described using Verilog HDL and synthesized as a controller with DC (Synopsys tool) with 0.5um standard library cells. This controller was floor-planned and routed using DSM module in Cadence. Its layout was automatically generated in this flow. Fig. 20 shows the layout.

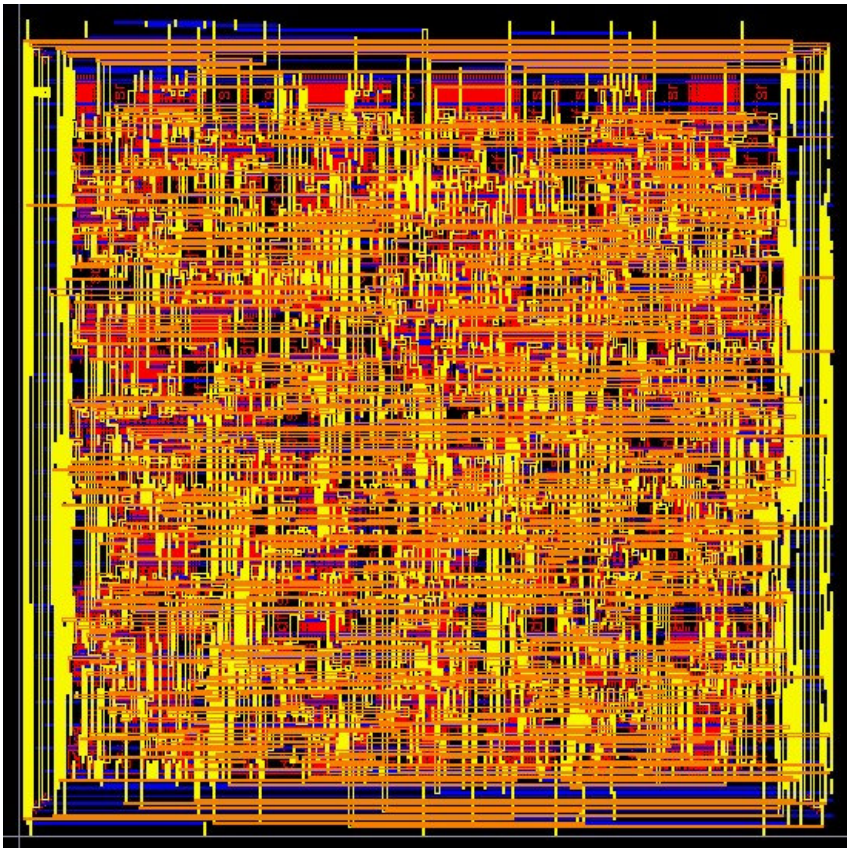


Fig.20 layout of the controller realizing bifurcation searching algorithm

V. System and Circuit Simulation Results

Bifurcation detection and branching parameter tuning algorithms are verified in MATLAB then transferred into synthesizable HDL codes using Finite State Machine. Digital logic part is in HDL codes while all analog circuits are in transistor-level. The main amplifier in Fig. 16 has been simulated with 65nm predicted CMOS process as well as 90nm-0.5um processes using either industrial BSIM3v3 models or predicted BSIM4 models. The whole system was simulated in a mixed-signal environment using Cadence tools.

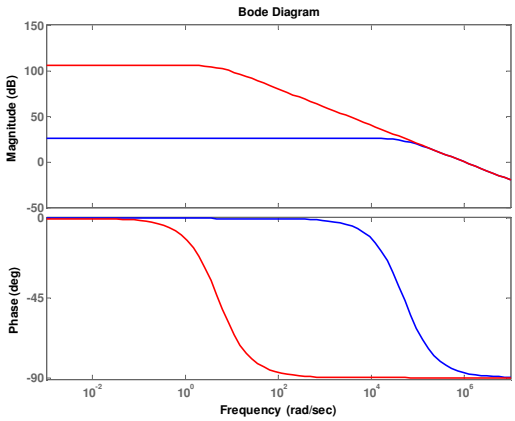


Fig. 21 frequency responses of the amplifier (pre-calibration and post calibration)

Fig. 21 shows the AC response of the positive feedback amplifier with an automatic-searched optimal control code Γ(0101110) (red) and an all-1 control code. As predicted by equation (21), more than 60dB gain enhancement was obtained with $\Delta = 0.001$.

Fig. 22 shows the automatic control-code searching procedure by the algorithm. Because of $\mu = \mu_{\min} + \Gamma \times \Delta$, bifurcation presents when Γ is large. After finishing branching parameter tuning, the final control code is the same as Γ(101110).

Γ	64	32	48	52	50	49	48
bifurcation	yes	no	no	yes	yes	yes	no

Fig. 22 optimal control code searching procedure

Fig. 23 illustrates DC transfer characteristics of this amplifier with two different codes. One can find that the bifurcation parameter-tuning algorithms boost the amplifier's output to a larger value than un-tuned part over all excitation range.

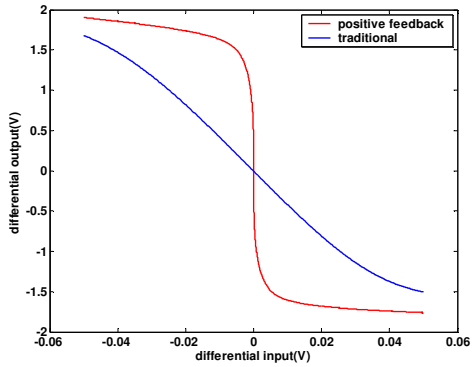


Fig. 23 DC transfer characteristics before/after tuning

Simulation results confirmed that the two-loop bifurcation parameter-tuning algorithm works in the same matter as we designed it and this algorithm found an optimal control code for the positive feedback amplifier. Furthermore, this algorithm is capable to detect more than 80dB gain in the bifurcation case that meets our specification.

VI. Conclusions

System dynamics of a CMOS positive feedback amplifier were analyzed and its nonlinear bifurcation behavior was discussed. The bifurcation leads to a new easy-to-realize detection method in the amplifier output due to memory effect. Thus bifurcation detection with pull-up/pull-down circuitry was introduced to reflect the amplifier's open-loop stability. Based on the bifurcation detection and programmable attenuation (functioning as bifurcation parameter), a positive feedback amplifier with self-calibration logic was introduced and implemented in digital CMOS technology. This method enhanced the amplifier DC gain dramatically while maintaining high power efficiency and minimizing hardware cost. Extending from traditional circuit design techniques, we developed a robust design method for high gain low-voltage compatible amplifiers using parameter dependent bifurcation in

dynamical systems. Circuit simulation results match analytical derivation well. Our method also makes it possible to use small feature size devices to construct high gain amplifiers with low parasitic. Low parasitic helps to enhance speed and reduce parasitic-related nonlinearity in systems such as Analog-to-Digital Converters.

This new design with low cost digital post-process techniques will enhance the stability and yield of the positive feedback amplifier dramatically. It will pave the way of industrial adoption of positive feedback amplifiers. Furthermore, our approach demonstrates the feasibility of high performance analog functionalities in standard digital CMOS. Thus our work will contribute to solve the difficult challenges in SOC as well as mixed-signal circuits and systems.

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CHAPTER 4. NEW LAYOUT STRATEGIES WITH IMPROVED MATCHING PERFORMANCE

Chengming He, Xin Dai, Hanqing Xing, Degang Chen

Abstract

In this paper, the systematic mismatch error in integrated circuits due to gradient effects is modeled and analyzed. Three layout strategies with improved matching performance are reviewed and summarized. The hexagonal tessellation pattern can cancel quadratic gradient errors with only 3 units for each device and has high area-efficiency when extended. Both the N^{th}-order circular symmetry patterns and N^{th}-order central symmetry patterns can cancel up to N^{th}-order gradient effects between two devices using 2^N unit cells for each one. Among these three techniques, the central symmetry patterns have the best-reported matching performance for Manhattan structures; the circular-symmetry patterns have the best theoretical matching performance; and the hexagonal tessellation pattern has high density and high structural stability. The N^{th}-order central symmetry technique is compatible to all IC fabrication processes requiring no special design rules. Simulation results of these proposed techniques show better matching characteristics than other existing layout techniques under nonlinear gradient effects. Specifically, two pairs of P-poly resistors using 2^{nd} and 3^{rd}-order central symmetry patterns were fabricated and tested. Less than 0.04% mismatch and less than 0.002% mismatch were achieved for the 2^{nd} and the 3^{rd}-order structures, respectively.

Key words: matching, symmetry, layout, and pattern

I. Introduction

In VLSI circuits, mismatch errors are the difference between two or more device parameters that are desired to be identical. Matching accuracy, to some extent, dominates the performance of analog and mixed-signal integrated circuits. For example, matching of sampling capacitors in switched-capacitor (SC) circuits directly affects the performance of pipelined/cyclic ADCs and SC filters. Matching characteristics of current mirrors play a key role in many applications [1, 2]. In modern communications circuits such as quadrature modulators, I/Q matching directly affects the image-rejection ratio, which is a key performance index. Matching in a differential amplifier limits reduction of even-order harmonics, especially the 2^{nd} order harmonic. Layout techniques to handle mismatch errors become more important to high-performance circuits design, since even a small amount of mismatch may easily hurt the performance of a precision circuit.

Over the years, great efforts have been made to the study of mismatch and layout strategies [3-6]. Previous studies show that the causes of mismatch can be categorized as systematic and random variations. The random variations are usually modeled by zero mean Gaussian distribution and tradeoffs can be made between area and matching accuracy [4]. The systematic variations are process dependent and usually modeled as spatial gradients in device parameters. The mismatch due to systematic variations may be at the same level of that of random variations [7]. If the random mismatch is reduced by increasing the area, the systematic mismatch becomes dominant. Furthermore, increasing area actually make the gradient effect more significant. Since mismatch due to systematic variations can cause performance degradation, it should be carefully handled and minimized.

Despite the widely recognized importance of matching, existing design and layout strategies dealing with the systematic mismatch are quite limited. Putting unit cells closely to each other reduces the gradient effect, but does not cancel it. The widely used common centroid layout pattern can only compensate for linear gradient [8]. Although the fully differential structure is robust to even-order harmonics, 2^{nd} order gradients can introduce 3^{rd}-order harmonics that fully differential structure cannot reduce. This error limits the dynamic range of some precision circuits. In this paper, three layout techniques capable of canceling mismatch errors due to high-order gradient effects are introduced. The N^{th}-order circular symmetry [6] and N^{th}-order central symmetry patterns [9] can cancel mismatch errors introduced by linear to N^{th}-order gradient effects, when each device uses 2^N unit cells. The hexagonal tessellation pattern [6] can cancel quadratic gradient effect with only 3 units for each device and has high area-efficiency. Among these three layout techniques, central symmetry patterns have the best matching performance for Manhattan structures; circular-symmetry patterns have the best theoretical matching performance; and the hexagonal tessellation pattern has high density and high structural stability with its honeycomb structure. The N^{th}-order central symmetry technique is compatible to all IC fabrication processes requiring no special design rules. These properties are proven by theoretical derivation and their matching performance is evaluated using MATLAB simulation.

The rest of the paper is organized as follows. In Section II, a general mathematical model of gradient effects is given. Section III describes three layout strategies and shows how they can cancel nonlinear gradient effects. Section IV gives the simulation results of the proposed layout strategies and some measurement results.

II. Gradient Modeling

A two dimensional polynomial function $p(x, y)$ can be used to model a parameter at the point (x, y). A parameter that has linear gradient can be modeled as

$$p_1(x, y) = G_1(x, y) + C, \tag{1}$$

where (x, y) is the coordinate of the point of interest, C is a constant, and

$$G_1(x, y) = g_{1,0}x + g_{0,1}y \tag{2}$$

is the linear gradient component of p. $g_{1,0}$ and $g_{0,1}$ are the linear gradient coefficients. Equation (1) can be easily extended to higher-order cases. Generally, a parameter that has up to n^{th}-order gradient components can be modeled as

$$p_n(x, y) = \sum_{j=1}^{n} G_j(x, y) + C, \tag{3}$$

where

$$G_j(x, y) = \sum_{k=0}^{j} g_{k,j-k}x^k y^{j-k} \tag{4}$$

is the j^{th}-order component. $g_{k,j-k}$'s are the j^{th}-order coefficients.

Now consider one of the unit cells composing a device, the parameter of the unit cell is the integral of the parameter value over the area of the unit cell. Since the area of the unit cell is usually small, the gradient effect over the unit cell is negligible and the parameter of the unit cell can be approximated by the parameter at a particular point P in the unit cell. Using the location of this point as the location of the unit cell, for a device composed of m unit cells located at $(x_1,y_1)\ldots(x_m,y_m)$, we can get the device's parameter as

$$P = \sum_{i=1}^{m} p_n(x_i, y_i), \tag{5}$$

where n is the highest order of the gradient effect. For two devices A and B, ideal matching is achieved if the mismatch error

$$\Omega(A,B) = P_A - P_B = 0. \tag{6}$$

Substituting x with $(x\text{-}x_0+x_0)$ and y with $(y\text{-}y_0+y_0)$ in (3), we get

$$p_n(x,y) = \sum_{k=1}^{n}\sum_{j=0}^{k} g_{j,k-j}(x-x_0+x_0)^j(y-y_0+y_0)^{k-j} + C, \tag{7}$$

which can be rewritten as

$$\begin{aligned} p_n(x,y) = &\sum_{j=0}^{n} g_{j,n-j}(x-x_0+x_0)^j(y-y_0+y_0)^{n-j} + \\ &\sum_{k=1}^{n-1}\sum_{j=0}^{k} g_{j,k-j}(x-x_0+x_0)^j(y-y_0+y_0)^{k-j} + C \end{aligned}. \tag{8}$$

Defining the 1st item to be I_1 and expending it gives

$$I_1 = \sum_{j=0}^{n} g_{j,n-j}\left(\left(\sum_{k=0}^{j}\binom{j}{k}x_0^{j-k}(x-x_0)^k\right)\times\left(\sum_{l=0}^{n-j}\binom{n-j}{l}y_0^{n-j-l}(y-y_0)^l\right)\right). \tag{9}$$

Equation (9) can be rewritten as

$$I_1 = \sum_{j=0}^{n} g_{j,n-j}(x-x_0)^j(y-y_0)^{n-j} + \sum_{j=0}^{n} g_{j,n-j}\sum_{k\ge 0, l\ge 0, k+l\le n-1} a_{k,l}(x-x_0)^k(y-y_0)^l, \tag{10}$$

where $\alpha_{k,l}$ is the coefficient of $(x\text{-}x_0)^k(y\text{-}y_0)^l$ assuming x_0 and y_0 constant. Notice that the order of the 2nd term in (8) and the 2nd term in (10) are both no greater than (n-1). That means (8) can be expressed in the form of

$$p_n(x,y)=\sum_{j=0}^{n} g_{j,n-j}(x-x_0)^j(y-y_0)^{n-j}+\sum_{i=1}^{n-1} G_i^{'}(x,y)+C^{'}, \tag{11}$$

where

$$G_i^{'}(x,y)=\sum_{j=0}^{i} g_{j,i-j}^{'} x^j y^{i-j} \tag{12}$$

has the same form as $G_i(x, y)$, but with different coefficients. And C' is a constant. Equation (11) shows that the center of nth order gradient can be moved from (0,0) where $G_n(x, y)=0$ to arbitrarily any point (x_0, y_0) so that $G_n(x-x_0, y-y_0)=0$, and this will only introduce lower order gradient components.

III. Three Layout Techniques Canceling High-Order Nonlinear Gradient

3.1 Nth-order central symmetry pattern

The central symmetrical layout pattern is for 1-1 matching between two devices. A description of the pattern is as follows:

i) The 1st order form of the pattern is just any common centroid pattern. Such as shown in Fig. 1(a) and (b). Common centroid layout pattern ensures the cancellation of linear (1st order) gradient error.

ii) The nth (n>1) order central symmetrical pattern can be defined in terms of the (n-1)st order pattern. The nth order pattern is composed of two n-1st order patterns symmetrical to a center C_n. There are two cases according to n's parity:

a) If n is odd, the unit cells of each device is central symmetrical around C_n. That means for each unit cell of device A at point P, there is another unit cell of device A at point P' and the middle point of segment PP' is exactly the symmetrical center C_n.

b) If n is even, the unit cells of the two devices in one of the n-1st order patterns should be interchanged so that the position of device A's unit cells are central symmetrical to device B's unit cells around C_n. That means for each unit cell of device A at point P, there is an unit cell of device B at point P' and the middle point of segment PP' is exactly the symmetrical center C_n. Fig. 2 and Fig. 3 show some high order (n>=2) central symmetrical layout patterns.

The following analysis will show how the central symmetrical layout pattern can cancel nonlinear gradient effect. Suppose both device A and device B has m unit cells.

i) If n=1, the parameter only has linear gradient effect. According to (5), the parameter of device A is

$$P_A = \sum_{i=1}^{m} p_1(x_{Ai}, y_{Ai}) = \sum_{i=1}^{m} (g_{1,0} x_{Ai} + g_{0,1} y_{Ai} + C). \tag{13}$$

Similarly, the parameter of device B is

$$P_B = \sum_{i=1}^{m} p_1(x_{Bi}, y_{Bi}) = \sum_{i=1}^{m} (g_{1,0} x_{Bi} + g_{0,1} y_{Bi} + C). \tag{14}$$

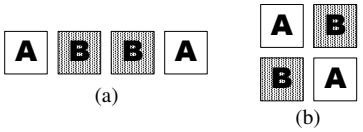


Fig. 1 examples of 1st order central symmetrical pattern

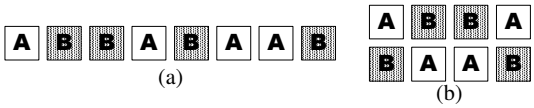


Fig. 2 examples of 2nd order central symmetrical pattern

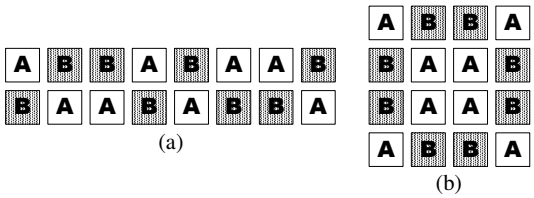


Fig. 3 examples of 3rd order central symmetrical pattern

The centroid of a device composed of m unit cells located at (x_i, y_i), i=1,2,…,m are defined as (x_c, y_c) where

$$x_c = \frac{1}{m}\sum_{i=1}^{m} x_i \,, \tag{15}$$

$$y_c = \frac{1}{m}\sum_{i=1}^{m} y_i \,. \tag{16}$$

From (13) ~ (16), it is not difficult to derive that (6) holds if and only if $x_{cA}=x_{cB}$ and $y_{cA}=y_{cB}$. This is why common centroid layout pattern can cancel linear gradient effect.

ii) Assume our proposed n[th]-order central symmetry layout can cancel mismatch from linear to the (n-1)[th]-order nonlinear gradient. Then if n>1, since the higher order pattern are constructed by duplicating lower order patterns, the number of unit cells of each device, m, must be an even number. Now consider the two cases according to n's parity:

If n is odd

Consider device A, according to the layout pattern, for a unit cell A_i at (x_{Ai}, y_{Ai}), there must be another unit cell A_{m-i} at (x_{Am-i},y_{Am-i}) which meets x_{Ai}-x_{Cn}=x_{Cn}-x_{Am-i} and y_{Ai}-y_{Cn}=y_{Cn}-y_{Am-i}. Then for any $0 \le j \le n$,

$$(x_{Ai} - x_{Cn})^j (y_{Ai} - y_{Cn})^{n-j} = -(x_{A,m-i} - x_{Cn})^j (y_{A,m-i} - y_{Cn})^{n-j}. \quad (17)$$

Choosing x_0 and y_0 in (11) to be x_{Cn} and y_{Cn} and substituting (11) to (5) gives

$$P_A = \sum_{i=1}^{m} \sum_{j=1}^{n-1} (G_j'(x_{Ai}, y_{Ai}) + C'). \quad (18)$$

Since unit cells of device B have the same central symmetry property, we get

$$P_B = \sum_{i=1}^{m} \sum_{j=1}^{n-1} (G_j'(x_{Bi}, y_{Bi}) + C'). \quad (19)$$

Equations (18) and (19) give

$$P_A - P_B = \sum_{i=1}^{m} \sum_{j=1}^{n-1} (G_j'(x_{Ai}, y_{Ai}) - G_j'(x_{Bi}, y_{Bi})). \quad (20)$$

This means the mismatch due to the n^{th} order gradient effect has been cancelled.

If n is even

According to the layout pattern, for an A's unit cell A_i at (x_{Ai}, y_{Ai}), there is a B's unit cell B_i at (x_{Bi}, y_{Bi}) which meets x_{Ai}-x_{Cn}=x_{Cn}-x_{Bi} and y_{Ai}-y_{Cn}=y_{Cn}-y_{Bi} . Then

$$(x_{Ai} - x_{Cn})^j (y_{Ai} - y_{Cn})^{n-j} = (x_{Bi} - x_{Cn})^j (y_{Bi} - y_{Cn})^{n-j}. \quad (21)$$

Choosing x_0 and y_0 in (11) to be x_{Cn} and y_{Cn}, and then substitute (11) to (5) gives

$$P_A = \sum_{i=1}^{m}(\sum_{j=0}^{n} g_{j,n-j}(x_{Ai} - x_{Cn})^j (y_{Ai} - y_{Cn})^{n-j} + \sum_{j=1}^{n-1}(G_j^{'}(x_{Ai}, y_{Ai}) + C') \quad (22)$$

and

$$P_B = \sum_{i=1}^{m}(\sum_{j=0}^{n} g_{j,n-j}(x_{Bi} - x_{Cn})^j (y_{Bi} - y_{Cn})^{n-j} + \sum_{j=1}^{n-1}(G_j^{'}(x_{Bi}, y_{Bi}) + C'). \quad (23)$$

Subtracting (23) from (22) still results in (20).

So the mismatch due to the n^{th} order gradient effect is cancelled for any n>1. Since the n^{th} order layout pattern is built from the n-1^{st} order layout pattern, which can cancel the first to the $(n-1)^{th}$ order gradient effect, the n^{th} order pattern should preserve this property and thus capable of canceling from the linear to the n^{th} order gradient.

Following this induction approach, it is proven that the N^{th}-order central symmetry layout technique can cancel from 1^{st} up to n^{th} order gradient effect.

3.2 N^{th} order circular symmetry pattern

The circular symmetry layout pattern is initially proposed for 1-1 matching between two devices. However, theoretical analysis suggests this layout pattern is capable for multiple devices' matching. A description of the pattern is as follows (each unit cell is modeled with a single point):

A desired device is composed with 2^n unit cells and their centers are located on a circle with an arbitrary center (x_0, y_0). The coordinates of these centers are defined in

$$\{X_i \mid (x_0 + \rho\cos\theta_i, y_0 + \rho\sin\theta_i), i = 1,...,2^n\}, \quad (24)$$

$$\{\theta \mid \theta_i = \theta_0 + (i-1)\frac{2\pi}{2^n}, i = 1,...,2^n\}. \quad (25)$$

Fig. 4 illustrates a second order circular symmetry patterns. The following analysis will show how the circular symmetry layout pattern can cancel nonlinear gradient effect. Using the gradient model (1)-(4), the effect of gradient on a point A_i can be expressed as (26)

$$p_n(A_i) = p_n(x_0 + \rho\cos\theta_i, y_0 + \rho\sin\theta_i) \tag{26}$$

and the total effect can be expressed by equation (27)

$$P_A = \sum_{i=1}^{2^n} p_n(A_i)\,. \tag{27}$$

Using trigonometry theory, we can use equation (28)

$$p_n(A_i) = g_0(x_0, y_0, \rho) + \sum_{j=1}^{n} g_j(x_0, y_0, \rho)\sin(j\theta_i + \phi_j) \tag{28}$$

to represent (26) with appropriate coefficients. The coefficients are determined by those in equations (1)-(4).

Thus we can extend equation (27) to (29)

$$\begin{aligned} P_A &= 2^n g_0(x_0, y_0, \rho) + \sum_{i=1}^{2\wedge n}\sum_{j=1}^{n} g_j(x_0, y_0, \rho)\sin(j\theta_i + \phi_j) \\ &= 2^n g_0(x_0, y_0, \rho) + \sum_{j=1}^{n} g_j(x_0, y_0, \rho)\sum_{i=1}^{2\wedge n}\sin(j\theta_i + \phi_j) \end{aligned}\,. \tag{29}$$

Define $$vP_j = g_j(x_0, y_0, \rho)\sum_{i=1}^{2\wedge n}\sin(j\theta_i + \phi_j)\,. \tag{30}$$

Then we will get

$$P_A = 2^n g_0(x_0, y_0, \rho) + \sum_{j=1}^{n} vP_j\,. \tag{31}$$

We will show $vP_j = 0$ using the well known equality $\sin(\theta + 2k\pi + \pi) + \sin\theta = 0$. Because $\{\theta \mid \theta_i = \theta_0 + (i-1)\frac{2\pi}{2^n}, i = 1,...,2^n\}$, for $j \le n$,

$$\sum_{i=1}^{2\wedge n} \sin(j\theta_i + \phi_j) = \sum_{i=1}^{2\wedge n} \sin[j\theta_0 + j(i-1)\frac{2\pi}{2^n} + \phi_j] \ . \tag{32}$$

It is not apparent that equation (32) is identical to zero. However, if *j* is odd, it is easy to show $\theta_{i+2^{n-1}} - \theta_i = j\pi, i = 1,2,\cdots,2^{n-1}$. At such a case, $vP_j = 0$. If *j* is even, we can express $j = 2^m k, k \ is \ odd$. It is easy to show that $\theta_{2^{n-m-1}+i} - \theta_i = k\pi$. $\{\theta \mid \theta_i = \theta_0 + (i-1)\frac{2\pi}{2^n}, i = 1,...,2^n\}$ can be grouped to 2^m exclusive and complete sub sets. At both cases, $vP_j = 0$ .Thus

$$P_A = 2^n g_0(x_0, y_0, \rho) . \tag{33}$$

We call the pattern of $A_i, i = 1,2,\cdots,2^n$ an n[th]-order circular symmetry pattern. One of the most important properties of this n[th] order circular symmetry pattern is **rotation-invariance**. This has been shown in our derivations since θ_0 can be any value. Mathematically we could place multiple sets of the n[th]-order circular symmetry pattern in the same circle. Thus it is capable of achieving matching among multiple devices. Multiple devices' matching property may have significant advantages in certain applications.

Thus, we have demonstrated and proven a layout pattern which will sufficiently cancel mismatch due to linear gradient and up to the n[th] order nonlinear gradient. It may cancel some higher order nonlinear gradient too. Although the derivations are based on point-

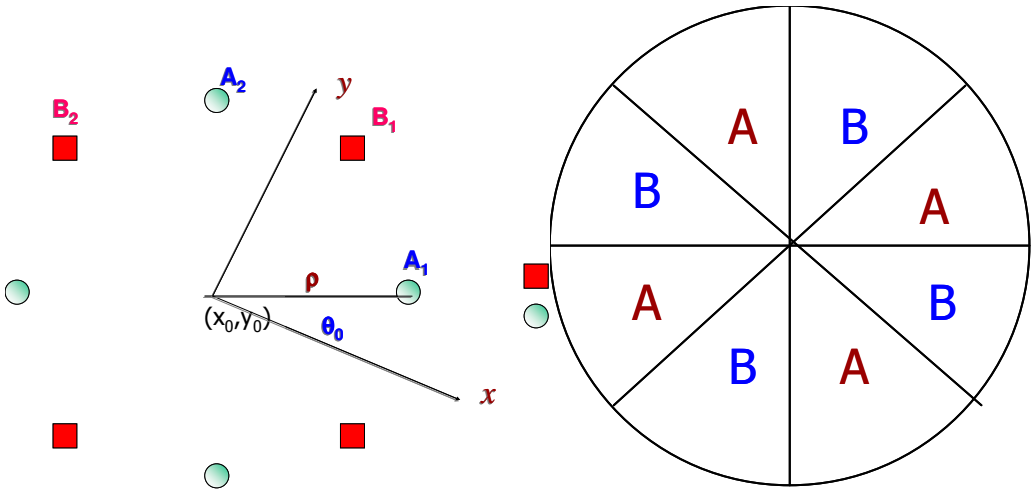
represents, the conclusion can be applied to a region. Construction of the N^{th} order circular symmetry patter would be as following:

a) build a unit cell.

b) place 2^{n+1} unit cells around a center (rotating the unit cell), the angle between adjacent unit cells to the center is $\pi / 2^n$

c) connect the alternative cells together and form two devices. As shown in Fig. 4b, A and B are matching up to the quadratic gradient.

It is worth to mention the common centroid layout and the 1^{st} order circular symmetry layout pattern. With some derivations, it will be shown that the device parameter would be a function independent of ρ. That just confirms the 1^{st} order circular symmetry pattern is a special common-centroid pattern. In other words, the common-centroid layout is an extended version of the first-order circular symmetry layout pattern.



(a) (b)

Fig. 4 a 2^{nd}-order circular symmetry pattern

3.3 Hexagonal Tessellation

Hexagon, the basic cell of bee nest, has wide applications in communication, architecture, chemical engineering and so on because of its high mechanical strength, high spatial efficiency. We will show hexagon also is the most concise layout pattern that can cancel linear and quadratic gradient completely. Furthermore, we can extend hexagon to construct the hexagonal tessellation pattern easily without space-waste.

Figure 5a shows a hexagon. The coordinates of the six vertexes $\{A_{i,}B_i, i=1,2,3\}$ can be annotated as

$$\{A_i, B_i \mid (x_0+\rho\cos\theta_i, y_0+\rho\sin\theta_i), i=1,2,3\},$$

$$\{\theta \mid \theta_i = \theta_0 + (i-1)\frac{2\pi}{3} + \frac{\pi}{3}a, i=1,2,3\}\ a=1:A;0:B. \tag{34}$$

For a quadratic gradient (n=2 in equation 5), we can prove that the total gradient is not related to θ_0. This is illustrated as equation (35)

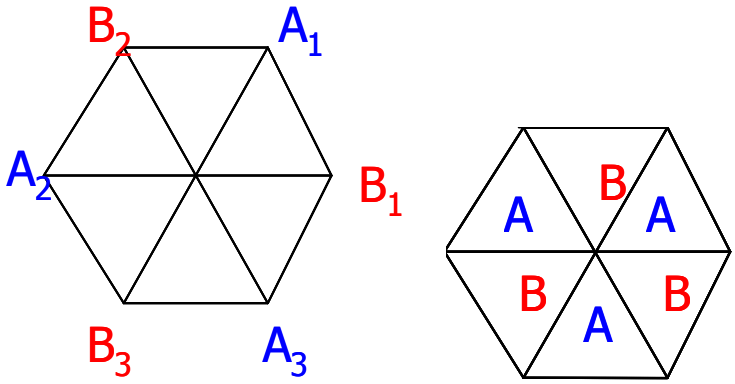
$$\sum_{i=1}^{3} p_2(A_i) = g(x_0, y_0, \rho) \tag{35}$$

and equation (36)

$$\sum_{i=1}^{3} p_2(B_i) = g(x_0, y_0, \rho). \tag{36}$$

Thus the gradient effects on both A and B are the same. Mismatch due to linear to quadratic gradient between A and B is cancelled.

Fig. 5b shows a divided hexagon. There are six triangles. Assuming each triangle is represented by its center of gravity, the six centers of gravity will form a hexagon in the fashion as that in Fig. 5a. Thus the As and Bs in Fig. 5b match with each other.



(a) (b)

Fig. 5 hexagonal matching pattern

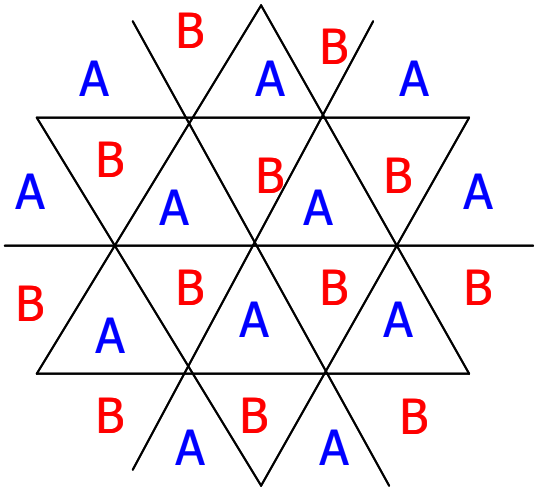


Fig. 6 hexagonal tessellation

As shown in Fig. 6, a hexagon can be extended and filled with As and Bs in a way that forms a honeycomb structure. The layout pattern shown in Fig. 6 is named as hexagon tessellation. Because honeycomb structure is well known for its compact, high area-efficient

and low sensitive to stress, the hexagon tessellation pattern would also have excellent matching even under external stress and no area would be wasted.

IV. Evaluation of Three Layout Patterns and Measurement Results

4.1 Evaluation of proposed layout patterns through simulations

To evaluate the performance of the proposed layout techniques, we did MATLAB simulations on some of the existing layout patterns and the proposed patterns under different gradient effects. The layout patterns we chose are 1^{st} order (common centroid) ~ 5^{th} order central symmetrical pattern (Fig. 7 (a) ~ (e)), 2^{nd} order circular symmetry pattern (Fig. 7(f)) and hexagonal (Fig. 7(g)). Same total device area is assigned for each layout pattern and every unit cell is a rectangle. If triangle unit cell is used, the 2^{nd} order circular symmetry pattern and hexagonal tessellation pattern shown in Fig. 6 should have much better matching performance. Up to 5^{th} order gradient are generated for simulation. When we study the effect of k^{th} order gradient, we use k^{th}-order polynomial terms plus constant 1

$$G_k(x,y) = 1 + a\sum_{i=0}^{k} x^i y^{k-i}, a << 1. \tag{37}$$

The simulation results are summarized in table 4-1 where mismatch is defined by (38)

$$\Omega = 2\times\left|\frac{p_A - p_B}{p_A + p_B}\right|\times 100\%. \tag{38}$$

Table 4-1 Simulation results of different layout patterns

Mismatch (%)	Highest Order of Gradient				
	1st	2nd	3rd	4th	5th
Fig. 7 (a)	0	2.77	5.22	7.43	10.39
Fig. 7 (b)	0	0	0.24	0.87	1.70
Fig. 7 (c)	0	0	0	0.01	0.068
Fig. 7 (d)	0	0	0	0	0.0023
Fig. 7 (e)	0	0	0	0	0
Fig. 7 (f)	0	0	0	0.026	0.18
Fig. 7 (g)	0	0	0.26	0.50	2.24
Fig. 4 (b)	0	0	0	0.017	0.12
Fig. 5 (b)	0	0	0.17	0.32	1.48

Simulation results show that for n=1,…,5, the n^{th} order central symmetrical pattern can cancel up to nth order gradient effect, which is consistent with the previous analysis. Furthermore, the hexagonal is the efficient layout to cancel up to 2nd order gradient. The 2nd order circular symmetry pattern cancels up to the 3rd order gradient, instead of only the 1st and 2nd order gradient as mentioned in [6].In this pattern, the placement of the unit cells of a device is central symmetrical around the center of the circle. According to the analysis in section II and III, when n=3 is odd, as long as it cancels up to 2nd order gradient, it would also cancel the 3rd order gradient. This also implies that the $(2n)^{th}$-order circular symmetry pattern would cancel $(2n+1)^{th}$-order nonlinear gradient. Compared with these layout techniques, the central symmetrical layout is more area efficient and flexible in cell

placement. And it is easy to be extended to high order cases for cancellation of any high order gradient.

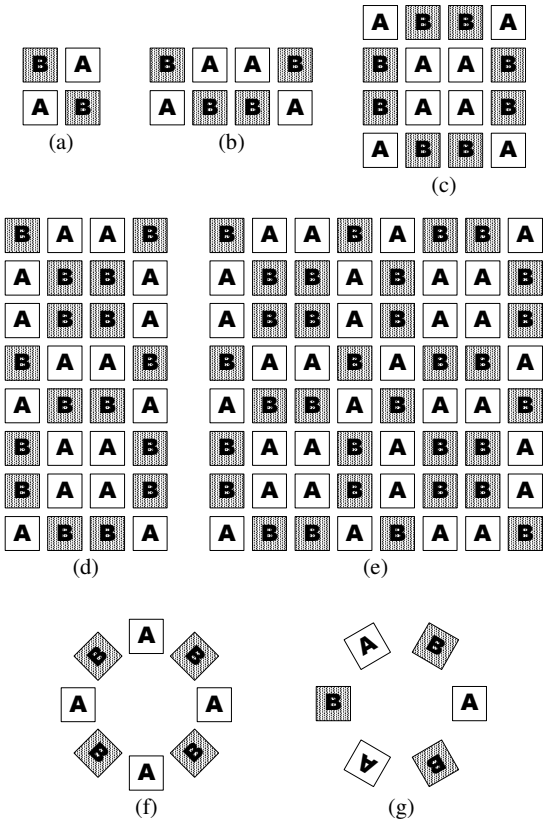


Fig. 7 layout patterns used in simulation

Our layout strategies do not make use of process information and is independent of what causes the gradient errors. Therefore, the experimental results only depend on the actual gradient errors present, but they should be independent of the process used. This is important because process-independent matching property makes our novel layout patterns usable in all available process technologies.

4.2 Validation of proposed layout techniques through measurements

The proposed N^{th}-order central symmetry pattern has been verified on silicon. Although transistor or capacitor matching might be more interesting, resistors are used in our

silicon implementation due to two main reasons. First, the measurement of transistor or capacitor matching is significantly more involved than the measurement of resistor matching. We want to separate measurement error from gradient-induced mismatch error. Since this paper is the first time the layout strategy is introduced, we wanted to make sure that we were only comparing the influence of layout on matching errors and measurement quality can be easily ensured. Second, at the time of designing the circuit prototype at Silicon Labs Inc, a passive complex polyphase filter is specified to achieve better than 70dB image rejection ratio (IRR). The complex polyphase filter is composed of resistors and capacitors. According to [10], this IRR requires better than 64dB matching performance in both resistors and capacitors. Since for the same level of accuracy requirement, capacitor matching is significantly easier than resistor matching, a satisfactory capacitor realization has been found at the time, achieving the required 64dB-matching, whereas a solution for achieving 64-dB matching in resistors remained challenging. For these two reasons, we have selected resistor matching as the first vehicle to demonstrate the new layout strategies. Transistor matching or capacitor matching can be a future study topic. We believe that our analysis, simulations and measurement data are sufficiently to demonstrate the effectiveness of improving matching using our proposed new layout strategies.

Based on random mismatch data on TSMC characterization reports, a specific area was allocated to each resistor. The proposed N^{th}-order central symmetry layout pattern was chosen. In order to reduce complexity of layout work, the 2^{nd}-order and 3^{rd}-order pattern were adopted and fabricated in 0.13 um CMOS process. P+ type unsilicided poly is used to construct the designated resistors due to its low temperature coefficients and low nonlinearity. For the 2^{nd}-order pattern as shown in Fig. 8a, one resistor was constructed by paralleling 4

identical resistor-units. Each had an area of 1/8 of the total area. For the 3rd-order pattern shown in Fig. 8b, each resistor was constructed in a parallel-series connection combining 8 unit cells in the 3rd-order central symmetry pattern.

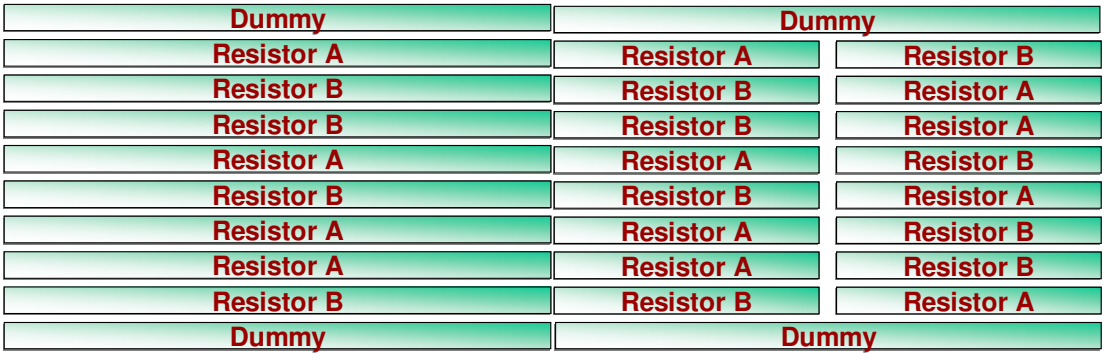


Fig. 8 two precisely-matched resistor pairs: a) 2nd order; b) 3rd order

4.2.1 Measurement setup

1) Resistance measurement

A resistor nominally has two terminals and is measured directly from these two terminals with an Ohmmeter. However, as shown in Fig. 9, wire-resistance would be included in this measurement. For a precise resistance measurement, it requires new measuring method.

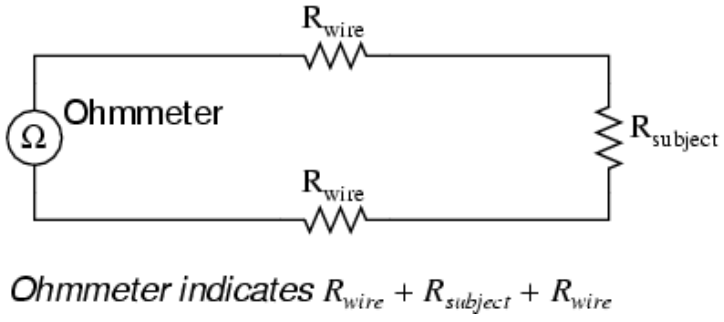
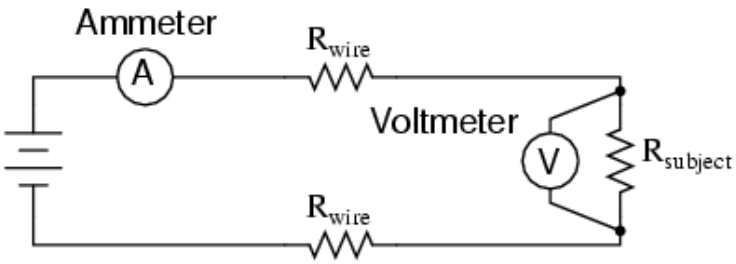


Fig 9 basic method of measuring resistance

It has been shown that we can use Kelvin resistance measurement method. Illustrated in Fig. 10, it involves the use of both an ammeter and a voltmeter. Ohm's Law defines that resistance is equal to voltage divided by current (R = V/I). Thus, we should be able to determine the resistance of the subject component if we measure the current going through it and the voltage drop across it.



$$R_{subject} = \frac{\text{Voltmeter indication}}{\text{Ammeter indication}}$$

Fig. 10 Kelvin resistance measurement method

Thus this two-terminal resistor is extended to a four-terminal Kelvin resistor, as shown in Fig. 11.

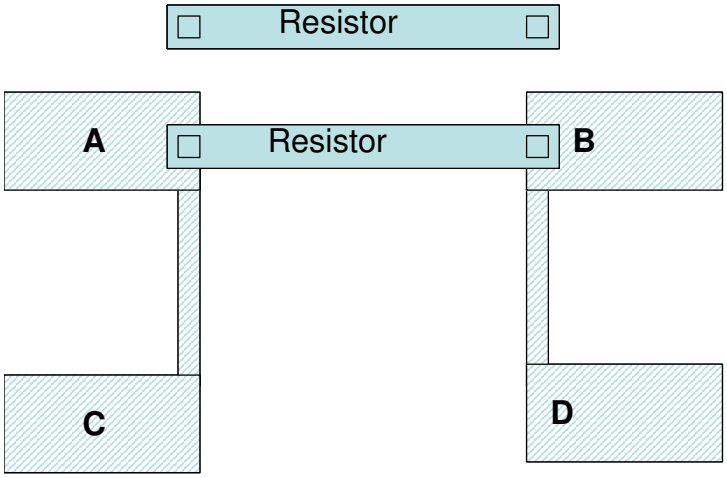


Fig.11 Four-terminal resistor simplifying precise resistance measurement

2) Measurement of resistance-matching performance

In our research, we are mainly interested in studying matching performance. Thus we can use alternative ways to avoid measuring resistance. Instead, a voltage divider is constructed and voltages drops across these two resistors are measured. Kelvin resistor structure is still adopted because it removes the wire resistance effect. Fig. 12 illustrates this layout.

The test structures are fabricated and packaged. A special socket and a custom-designed printed-circuit board were designed to support this package. A DC power supply of HP E3611A was connected to N1 and N4 nodes while voltage drops across the two resistor-pairs were measured by a multi-channel sampling system with more than 16-bit accuracy provided by National Instruments. Measurements are automated with National Instruments' software LabView.

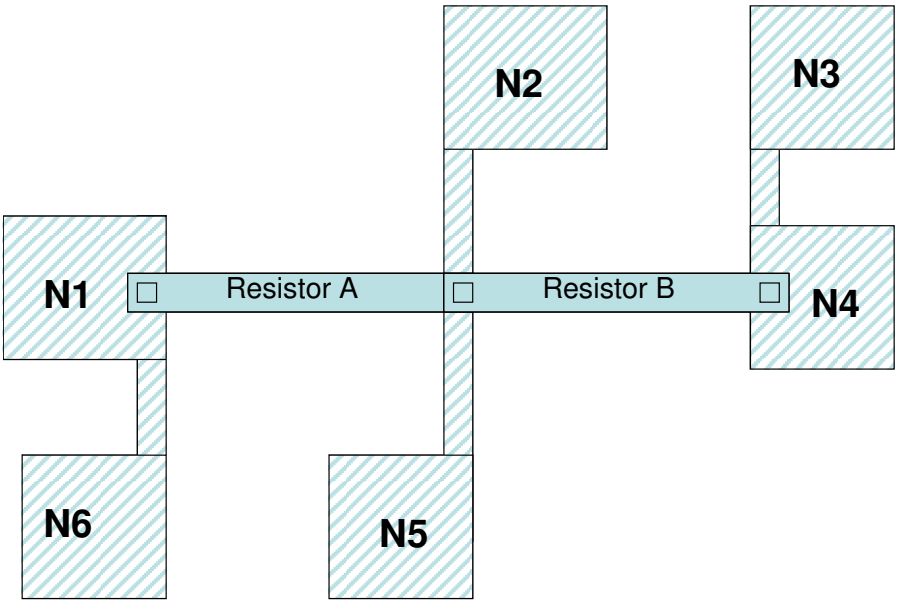


Fig.12 resistive voltage divider with Kelvin terminals

Because noise and socket-landing could affect measurement results, multiple measurements with single-landing and multiple-landing are both applied for the same resistor, raw data are processed to eliminate wrong data, and finally processed-data are statistically analyzed.

In order to have a high confidence of matching measurements, sufficiently large number of devices should be tested. In our project, a few wafers from the same run were used and more than 100 dies were measured. Table 4-2 and table 4-3 illustrate the statistical measurement results.

Table 4-2 matching performance of one resistor-pair in 2nd order central symmetry pattern

	Same resistor pair with single-landing	Same resistor pair with multiple-landing	Large samples
Mean	0.077%	0.077%	0.04%
Standard deviation	0.0018%	0.0016%	0.034%

Table 4-3 matching performance of one resistor-pair in 3rd order central symmetry pattern

	Same resistor pair with single-landing	Same resistor pair with multiple-landing	Large samples
Mean	0.02008%	0.0205%	0.003%
Standard deviation	0.0017%	0.0011%	0.038%

4.2.2 Discussion of this measurement

Table 2 and 3 suggest that our proposed 2nd order central symmetry pattern has better than 400ppm (0.04%) systematic mismatch and the 3rd order one has better than 30ppm systematic mismatch. This confirms that our proposed Nth-order central symmetry patterns are effective in improving matching performance.

However, the proposed 3rd order pattern has more random mismatch than the 2nd order one. This can be explained partly by contact and wire-connection mismatches. The 3rd order pattern would have more contacts and more interconnections than the 2nd order one. According to foundry data, contacts have larger standard deviations than core-resistor.

Furthermore, as table 1 and 2 show, measurement with single-landing has an error less than 0.0018%, measurement with multiple-landing has an error of 0.0016%. This suggests equipments have an accuracy of less than 20ppm. This is negligible comparing to 340-380ppm of the random mismatch in these resistor pairs.

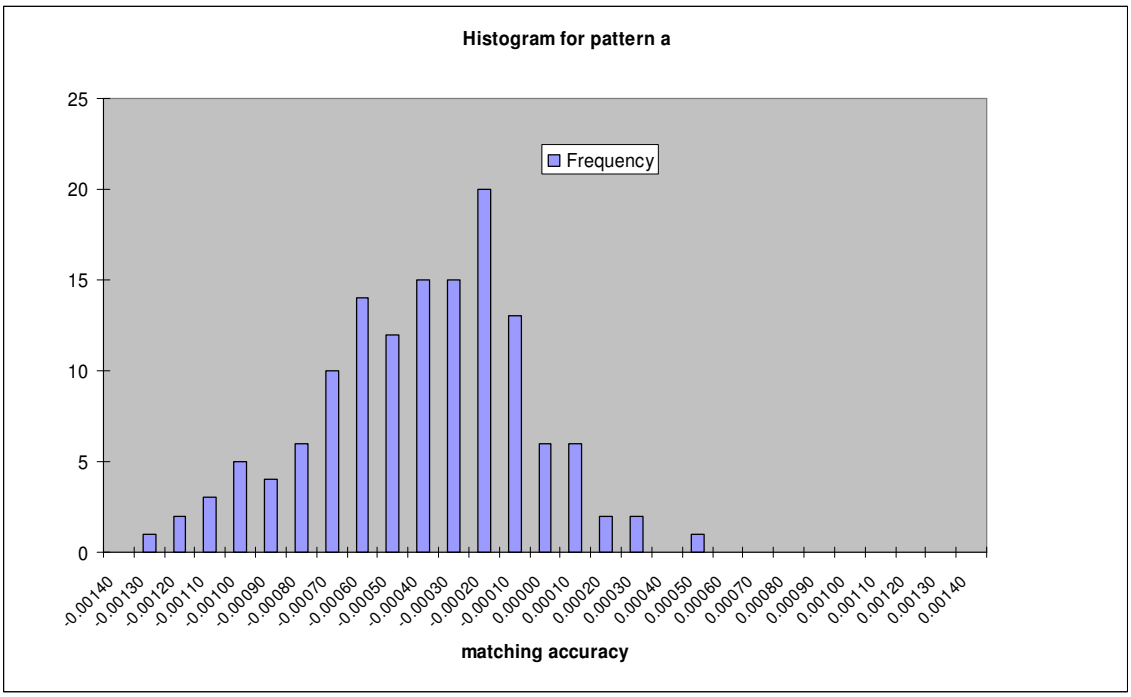
These two tables also suggest that multiple landing would reduce some standard deviation. This is consistent with random noise properties. Ideally we like to measure many times for the same resistor-pair to minimize noise effect. However, noise error could be ignored comparing to equipment accuracy and designated matching performance.

On the other hand, we assume the equipments have no systematic offset thus the equipments would not affect measured mean values. So this measurement of systematic error is accurate within equipment accuracy.

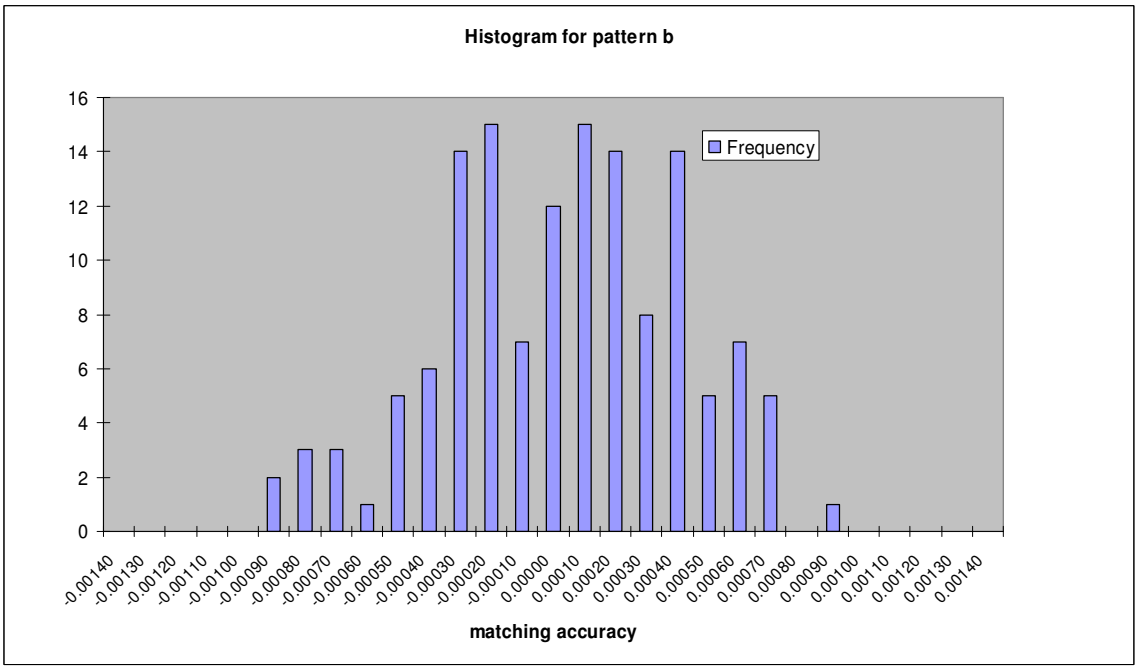
Fig. 13 illustrates the measured histogram plots. It is clear that pattern b) is more symmetric around 0 while pattern a) is somewhat biased toward negative residue which we believe is caused by high order gradients. Each has a standard deviation in consistence with

TSMC data. If we use 64dB as the decision boundary, we would achieve 84% yield using pattern a) and 91% yield using pattern b). If we use 60dB matching as the decision boundary, yield is 94% using pattern a) and 100% using pattern b). From these data, it is clear that the systematic error due to linear and nonlinear gradient have been reduced by the proposed strategy to a level that they are dominated by random errors. To further reduce mismatch and/or improve yield, the total area allocation needs to be increased.

It would be more persuasive if we compare traditional layout techniques. Even though we did not draw any traditional layout patterns by ourselves, we learned that most untrimmed passive polyphase filters typically have an IRR smaller than 40dB [11, 12]. This low IRR is most likely limited by resistor matching since capacitor matching is much easier. Thus, our measurement results would be sufficient to confirm the matching improvement using our proposed high-order nonlinear gradient canceling layout patterns.



a)



b)

Fig. 13 histogram plots of the 2nd order and 3rd order resistor-pairs

V. Conclusions

This paper modeled and analyzed the systematic mismatch due to linear and nonlinear gradient effects. Based on the analysis, we proposed three layout techniques capable of canceling mismatch errors due to high-order gradient effects. The N^{th}-order circular symmetry [6] and N^{th}-order central symmetry patterns [9] can cancel mismatch from linear to the n^{th}-order gradient between two devices by using 2^n unit cells for each one; the hexagonal tessellation pattern [6] can cancel quadratic gradient with only 3 units for each device and has high area-efficiency. Among these three layout techniques, central symmetry patterns have the best reported matching performance for Manhattan structures; circular-symmetry patterns have the best theoretical matching performance; hexagonal tessellation pattern has high density, high structural stability with its honeycomb structure. The N^{th}-order central symmetry technique is compatible to all IC fabrication processes requiring no special design rules. All layout patterns have been mathematically proved and verified through simulation. Testing results of the proposed N^{th}-order central symmetry layout pattern confirmed our analysis and simulation.

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CHAPTER 5. ACCURATE CLOSED-LOOP LINEARITY ESTIMATION USING AMPLIFIERS' OPEN-LOOP DC TRANSFER

Chengming He, Le Jin, Hanjun Jiang, Degang Chen, Randall Geiger

***Abstract*:** Linearity is a major specification for both open-loop and closed-loop amplifiers. However, it is easier to simulate an open-loop amplifier. Especially, it is simple and time-saving to get the DC transfer characteristic for a high-gain amplifier. Based on the DC transfer, a simple equation showing the lower-bound of achievable low-frequency total harmonic distortion is demonstrated.

I. Introduction

A characteristic of development in the semiconductor industry has been that the dimensions of new devices and the threshold voltages required to drive them have been reduced continuously. With these developments, the performance of transistors becomes nonlinear. Under low supply voltage, the need for high gain and a large output swing in amplifiers forces designers to exploit the performance of transistors and to design circuits working in strongly nonlinear regions. Although engineers make great effort to improve the linearity of amplifiers, they cannot eliminate the non-linearity due to the intrinsic characteristics of semiconductors. Actual open-loop amplifiers always have nonlinear transfer characteristics, especially for positive feedback amplifiers. Such devices show highly nonlinear open-loop DC transfer characteristics. Although feedback improves linearity in the closed-loop configurations, the exact relationship of the open-loop DC transfer and closed-loop linearity is unknown. [1][2][3]

It is possible to run transient simulation, sample a voltage of interest, and run Fourier transformation to get linearity information, mainly harmonic distortion and total harmonic distortion. However, such a procedure is time consuming. It is preferred to estimate the closed-loop linearity (THD) accurately using the open-loop DC transfer. [4]

Section 2 introduces a simple amplifier model with a known DC transfer that gives a very strong lower-bound total harmonic distortion value in the feedback configuration with different feedback factor. Section 3 discusses the effect of the introduction of feedback in a closed-loop configuration, which justifies that only odd-order harmonics exist both in the open-loop and closed-loop configurations if the DC transfer is an odd function.

II. A DC-Transfer Based Amplifier Model and Open-Loop Equivalent Gains

For large signal swing and global analysis, all operational amplifiers will work in the nonlinear state. The linear models for amplifiers are simple approximations to the real situation and only work well for small signal swing and local analysis. If circuits perform well, signal swing in the circuits can no longer be kept “small” compared with the supply voltage. A simple method is needed to estimate linearity performance before running time-consuming simulations and FFT processing.

The present research replaces the bottom-up method from transistor level for modeling nonlinear amplifier characteristics with a top-down method. Static behavior of an operational amplifier is described by the DC transfer characteristic in which voltage is used for both input and output.

II.1 An amplifier's DC transfer

Fig. 1 shows a typical DC transfer characteristic for an amplifier. As illustrated in Fig. 1, the input is denoted as x while the output is denoted as y. The DC transfer is described by an odd function expressed in equation (1)

$$y = f(x),$$

$$f(-x) = -f(x). \tag{1}$$

$f(x)$ will have properties such as

$$f'(x) > 0. \tag{2}$$

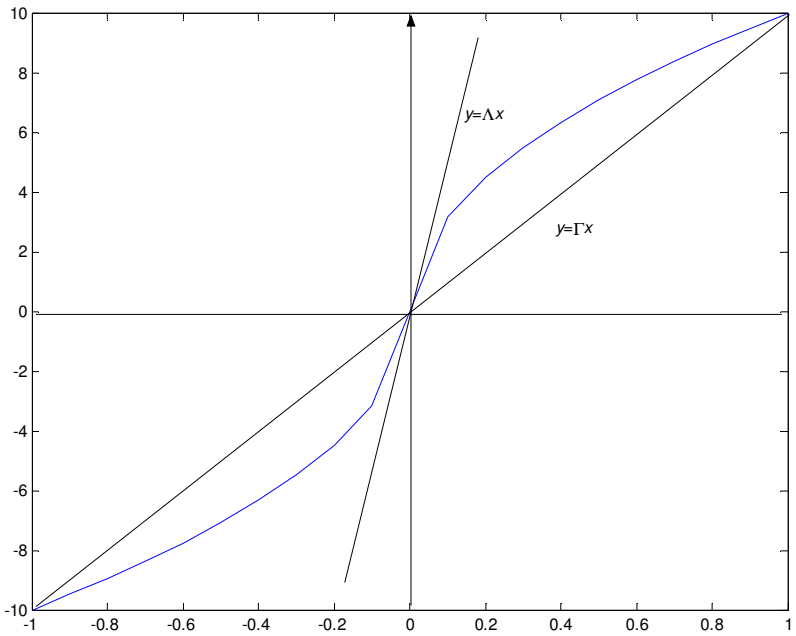

Fig. 1 DC transfer of a general amplifier

As shown in Fig. 1, in given output range $[0,V_O]$, the DC transfer $f(x)$ can be bound in a set $[\Gamma,\Lambda]$ such that

$$\Gamma x \le f(x) \le \Lambda x . \tag{3}$$

Depending on the output range, Γ is dependent on the output range, while Λ is the absolute value of the maximum slope. In the case of a practical amplifier, Λ is the absolute slope of the DC transfer at origin or the gain at the operating-point.

II.2 Linearity enhancement by feedback

Fig. 2 illustrates a conceptual feedback configuration using the amplifier described in Fig. 1.

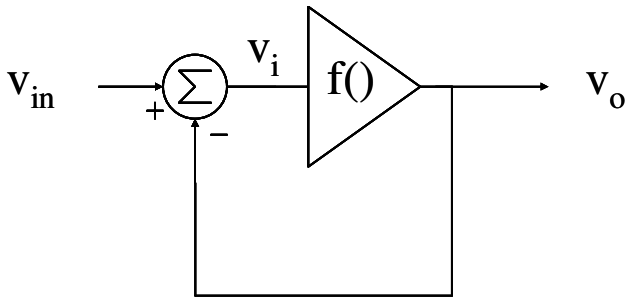

Fig. 2 Unit feedback amplifier

Assuming the amplifier has infinite bandwidth, it can be shown that

$$v_i = v_{in} - v_o , \tag{4}$$

and

$$v_o = f(v_i) = f(v_{in} - v_o) \tag{5}$$

With $v_i = v_{in} - v_o = f^{-1}(v_o)$, we can obtain $v_i v_o = f^{-1}(v_o) v_o \ge 0$.

If the amplifier shown in Fig. 1 has nonlinearity, feedback will improve linearity, but output would still be distorted. Assuming the input in the feedback amplifier is a single

frequency sinusoid waveform, the output and the internal node would be the sum of different harmonics with the same base frequency using the Fourier extension.

$$v_{in} = A\sin\omega t\,,\ A > 0\,,$$

$$v_o = \sum_{i=1}^{N} A_i \sin\omega_i t\,,$$

$$v_i = \sum_{i=1}^{N} B_i \sin\omega_i t\,. \tag{6}$$

Then equation (4) can rewritten as (7)

$$\sum_{k=1}^{\infty} B_k \sin k\omega t + \sum_{k=1}^{\infty} A_k \sin k\omega t = A\sin\omega t\,. \tag{7}$$

With the condition in equation (3), we can obtain

$$\sum_{k=1}^{\infty} B_k \sin k\omega t \sum_{k=1}^{\infty} A_k \sin k\omega t \geq \frac{1}{\Lambda}(\sum_{k=1}^{\infty} A_k \sin k\omega t)^2\,. \tag{8}$$

It is known that harmonics must be balanced in (7). This leads to equation (9)

$$B_1 = A - A_1\,, B_k = -A_k \ \text{ for } \ k \geq 2\,. \tag{9}$$

Equations (8) and (9) yield (10)

$$(A - A_1)A_1 - \sum_{k=2}^{\infty} A_k^2 \geq \frac{1}{\Lambda}\sum_{k=2}^{\infty} A_k^2\,, \tag{10}$$

and then (11)

$$AA_1 \geq (1+\frac{1}{\Lambda})\sum_{k=1}^{\infty} A_k^2\,. \tag{11}$$

Similarly, it can be shown that $AA_1 \leq (1+\frac{1}{\Gamma})\sum_{k=1}^{\infty} A_k^2$.

Because $AA_1 \geq (1+\frac{1}{\Lambda})\sum_{k=1}^{\infty} A_k^2$, it is true that $AA_1 \geq (1+\frac{1}{\Lambda})A_1^2 \geq 0$. This leads to an inequality (12)

$$A \geq (1+\frac{1}{\Lambda})A_1 \geq 0. \tag{12}$$

It is also true that inequality (13) is valid based on condition (3)

$$v_o f^{-1}(v_o) \geq \Gamma v_i^2,$$

$$\sum_{k=1}^{\infty} B_k \sin k\omega t \sum_{k=1}^{\infty} A_k \sin k\omega t \geq \Gamma(\sum_{k=1}^{\infty} B_k \sin k\omega t)^2. \tag{13}$$

By integrating (13) in a cycle, inequality (14) results

$$(A-A_1)A_1 - \sum_{k=2}^{\infty} A_k^2 \geq \Gamma\sum_{k=1}^{\infty} B_k^2 = \Gamma(A-A_1)^2 + \Gamma\sum_{k=2}^{\infty} A_k^2. \tag{14}$$

Thus we get $[(1+\Gamma)A_1 - \Gamma A](A-A_1) \geq (1+\Gamma)\sum_{k=2}^{\infty} A_k^2 \geq 0$, $(1+\Gamma)A_1 - \Gamma A \geq 0$, $A \leq (1+\frac{1}{\Gamma})A_1$.

Together with equation (12), we obtain $(1+\frac{1}{\Gamma})A_1^2 \geq AA_1 \geq (1+\frac{1}{\Lambda})\sum_{k=1}^{\infty} A_k^2$. Rearranging the terms yields a new inequality $(\frac{1}{\Gamma}-\frac{1}{\Lambda})A_1^2 \geq (1+\frac{1}{\Lambda})\sum_{k=2}^{\infty} A_k^2$. This is equivalent to

$$\frac{1}{(1+\frac{1}{\Lambda})}(\frac{1}{\Gamma}-\frac{1}{\Lambda}) \geq \frac{\sum_{k=2}^{\infty} A_k^2}{A_1^2}. \tag{15}$$

The inequality (15) sets the lower bound of low frequency linearity performance of a unity-gain feedback configuration. In addition to the unity-gain feedback configuration, it is worth considering a general feedback configuration with a feedback factor of β.

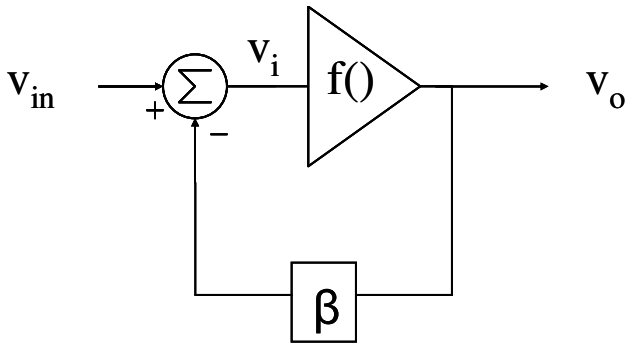

Fig. 3 a feedback configuration with a feedback factor β

Using voltage approach, we have

$$v_i = v_{in} - \beta v_o, \tag{16}$$

$$v_o = f(v_i) = f(v_{in} - \beta v_o). \tag{17}$$

Thus $v_i = v_{in} - \beta v_o = f^{-1}(v_o)$, $v_i v_o = f^{-1}(v_o) v_o$.

Using the same approach for a unity-feedback configuration, the result is distortion for the closed-loop configuration.

We assume the same stimulus is used in the feedback amplifier, $v_{in} = A\sin\omega t$, $A > 0$. The output and the internal node would be the sums of all possible harmonics, i. e., $v_o = \sum_{k=1}^{\infty} A_k \sin k\omega t$, $v_i = \sum_{k=1}^{\infty} B_k \sin k\omega t$.

By replacing corresponding terms equation (16) can be rewritten as (18)

$$\sum_{k=1}^{\infty} B_k \sin k\omega t + \beta \sum_{k=1}^{\infty} A_k \sin k\omega t = A\sin\omega t. \tag{18}$$

This suggests that $B_1 = A - \beta A_1$, $B_k = -\beta A_k$. Based on the condition (3), we can derive an inequality (19)

$$\sum_{k=1}^{\infty} B_k \sin k\omega t \sum_{k=1}^{\infty} A_k \sin k\omega t \geq \frac{1}{\Lambda} (\sum_{k=1}^{\infty} A_k \sin k\omega t)^2. \tag{19}$$

By integrating the two sides of the inequality (19) over time and replacing B_k by A_k's function, a new inequality is derived as (20)

$$(A-\beta A_1)A_1-\beta\sum_{k=2}^{\infty}A_k^2\geq\frac{1}{\Lambda}\sum_{k=1}^{\infty}A_k^2\ , \tag{20}$$

which is the same as (21)

$$AA_1\geq(\beta+\frac{1}{\Lambda})\sum_{k=1}^{\infty}A_k^2\ . \tag{21}$$

Similarly, $\sum_{k=1}^{\infty}B_k\sin k\omega t\sum_{k=1}^{\infty}A_k\sin k\omega t\leq\frac{1}{\Gamma}(\sum_{k=1}^{\infty}A_k\sin k\omega t)^2$ will lead to

$$AA_1\leq(\beta+\frac{1}{\Gamma})\sum_{k=1}^{\infty}A_k^2\ . \tag{22}$$

From (21) we can derive a new inequality

$$A\geq(\beta+\frac{1}{\Lambda})A_1\geq 0\ . \tag{23}$$

Because $|v_o|=|f(v_i)|\geq\Gamma|v_i|$, $v_o f^{-1}(v_o)=|v_o v_i|\geq\Gamma v_i^2$. Using the harmonic denotations yields inequality (24)

$$\sum_{k=1}^{\infty}B_k\sin k\omega t\sum_{k=1}^{\infty}A_k\sin k\omega t\geq\Gamma(\sum_{k=1}^{\infty}B_k\sin k\omega t)^2\ . \tag{24}$$

By integrating the inequality (24) over time, a new inequality (25) is the result:

$$(A-\beta A_1)A_1-\beta\sum_{k=2}^{\infty}A_k^2\geq\Gamma\sum_{k=1}^{\infty}B_k^2=\Gamma(A-\beta A_1)^2+\Gamma\beta^2\sum_{k=2}^{\infty}A_k^2\ . \tag{25}$$

The inequality is the same as inequality (26)

$$[A_1-\Gamma A+\Gamma\beta A_1](A-\beta A_1)\geq(1+\Gamma)\sum_{k=2}^{\infty}A_k^2\geq 0\ . \tag{26}$$

Because $A \geq (\beta + \frac{1}{\Lambda})A_1 \geq 0$, thus $A - \beta A_1 \geq 0$ thus $(1+\Gamma\beta)A_1 - \Gamma A \geq 0$.This suggests

$A \leq (\beta + \frac{1}{\Gamma})A_1$. Finally we derive a new inequality (27)

$$(\beta + \frac{1}{\Gamma})A_1^2 \geq AA_1 \geq (\beta + \frac{1}{\Lambda})\sum_{k=1}^{\infty} A_k^2 . \tag{27}$$

Inserting the first harmonic term in the left yields a new inequality (28)

$$(\frac{1}{\Gamma} - \frac{1}{\Lambda})A_1^2 \geq (\beta + \frac{1}{\Lambda})\sum_{k=2}^{\infty} A_k^2 . \tag{28}$$

Thus, it is possible to estimate a total harmonic distortion at low frequency as (29)

$$THD = \frac{\sum_{k=2}^{\infty} A_k^2}{A_1^2} \leq \frac{1}{(\beta + \frac{1}{\Lambda})}(\frac{1}{\Gamma} - \frac{1}{\Lambda}) \leq \frac{1}{\beta}(\frac{1}{\Gamma} - \frac{1}{\Lambda}) . \tag{29}$$

The expression (29) gives an upper bound of the largest possible low-frequency total harmonic distortion in an amplifier with the DC transfer in Fig. 1. As shown in Fig. 1, the coefficient Γ depends on the output level, the smaller the output, the closer to Λ.This means the THD will be small if there is a small output. For a linear amplifier, $\Gamma = \Lambda$ and there is no distortion at all.

Based on the inequality (29), a linearity index LI can be defined as

$$LI = \frac{\Gamma\Lambda}{\Lambda - \Gamma} . \tag{30}$$

Then the total harmonic distortion can be rewritten in decibel form

$$THD \leq -20\log LI - 20\log\beta . \tag{31}$$

For a unity-gain feedback configuration, MATLAB simulations confirmed this relationship. If the transfer is smooth, it is possible to estimate the THD more precisely as equation (32) [4]

$$THD = -20\log LI - 12(dB)\,. \tag{32}$$

MATLAB simulations confirmed these analyses and Table 5-1 summarizes the simulation results for the unity-gain feedback case.

Table 5-1 Estimated THD and simulated THD for close-loop amplifiers' output

Λ	Γ	LI	THD(est.) (dB)	THD(sim.) (dB)
10	9.99	10000	-92	-92.3
100	90.91	1000	-72	-72.31
100	98.04	5,000	-85.98	-86.3
100000	991	1001	-72.009	-72.0566
1000000	999	1000	-72	-72.056
100000	9,091	10000	-92	-92.043

III. Possible Harmonics in an Amplifier with Odd-Symmetry DC Transfer

Assume the amplifier has odd-symmetry DC transfer, as shown in Fig. 1, $f(v_i) = -f(-v_i)$. This suggests that at DC $v_o = \sum_{k=0}^{\infty} C_{2k+1} v_i^{2k+1}$. Assuming the amplifier has an infinite bandwidth and there is no delay in the feedback network (shown in Fig. 3), the result is $v_o(t) = \sum_{k=1}^{\infty} A_k \sin k\omega t$, $v_i(t) = \sum_{k=1}^{\infty} B_k \sin k\omega t$ when $v_{in}(t) = A\sin\omega t$. Then

$$v_o = \sum_{k=0}^{\infty} C_{2k+1} \left(\sum_{j=1}^{\infty} B_j \sin j\omega t\right)^{2j+1}. \tag{33}$$

In this expression, there are no even-odd harmonics; that is, $A_{2k} = 0$. Because $B_1 = A - \beta A_1, B_k = -\beta A_k$, $B_{2k} = 0$.

This analysis only applies to an amplifier with an infinite bandwidth. For a finite bandwidth amplifier, more thorough analyses are required.

To simplify the model, the amplifier is modeled such that it has infinite input impedance and a nonlinear output conductance (shown in Fig. 4). To model the odd-symmetric DC transfer, the output conductance is modeled by an even function $g_o(v_o) = g_o(-v_o) \geq 0$.

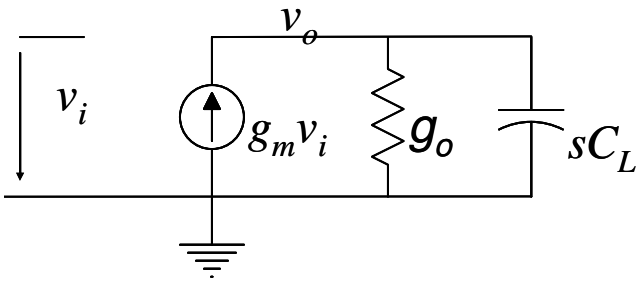

Fig. 4 a simple model of an amplifier

Thus at DC, $v_o = f(v_i) = \frac{g_m v_i}{g_o(v_o)} = \frac{g_m v_i}{g_o(f(v_i))}$ and

$$f(-v_i) = -\frac{g_m v_i}{g_o(f(-v_i))} = -\frac{g_m v_i}{g_o(-f(v_i))} = -\frac{g_m v_i}{g_o(f(v_i))} = -f(v_i). \tag{34}$$

This suggests there would be no even-order harmonic at DC.

When frequency goes high, a TDE would be introduced to study the dynamics of the feedback system. This is denoted as equation (35)

$$\frac{dv_o}{dt} = H * v_o + C(v_o)v_o + B\sin\omega t, \tag{35}$$

where $H = -\frac{\beta g_m}{C} < 0$, $B = \frac{g_m}{C} > 0$, $C(v_o) = -\frac{g_o(v_o)}{C} \le 0, \forall v_o$. Let $V = v_o^2$, $\dot{V} = 2v_o v_o^{'} = 2Hv_o^2 + 2C(v_o)v_o^2 + 2Bv_o \sin\omega t = 2[H + C(v_o)]v_o^2 + Bv_o \sin\omega t$. When $|v_o| > |\frac{B}{H}|$, $\dot{V} < 0$. Thus $(-|\frac{B}{H}|, |\frac{B}{H}|)$ is the positive invariant set of V. According to [5], a unique periodic solution $v_o(t) = v_o(t+T)$ exists for the non-linear differential equation. It is known that a periodic function can be expanded into Fourier series as (36) and (37)

$$v_o(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega t}, where \quad V_k = FS_k(v_o(t)), k \in Z, \tag{36}$$

$$C(v_o(t))v_o(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega t} . \tag{37}$$

Replacing the node voltage in (35) with the Fourier expansion yields (38)

$$\sum_{k=-\infty}^{\infty} jk\omega V_k e^{jk\omega t} = H \sum_{k=-\infty}^{\infty} V_k e^{jk\omega t} + \sum_{k=-\infty}^{\infty} C_k e^{jk\omega t} + \frac{B}{2j}(e^{j\omega t} - e^{-j\omega t}) , \tag{38}$$

which satisfies the harmonic balance equations:

$$\begin{aligned} jk\omega V_k &= HV_k + C_k, k \neq \pm 1 \\ j\omega V_1 &= HV_1 + C_1 + \frac{B}{2j} \\ j\omega V_{-1} &= HV_{-1} + C_{-1} - \frac{B}{2j} \end{aligned} . \tag{39}$$

Now assuming V_{2k}=0,

$$v_o(t) = \sum_{k=-\infty}^{\infty} V_{2k+1} e^{j(2k+1)\omega t} , \tag{40}$$

which can lead to (41)

$$\begin{aligned} & v_o(t + \frac{T}{2}) = -v_o(t) \\ & C(v_o(t + \frac{T}{2}))v_o(t + \frac{T}{2}) = -C(-v_o(t))v_o(t) = -C(v_o(t))v_o(t) \end{aligned} . \tag{41}$$

Thus, C_{2k}=0 since

$$\begin{aligned} C_{2k} &= \frac{1}{T}\int_0^T C(v_o(t))v_o(t)e^{-j2k\omega t}dt \\ &= \frac{1}{T}\int_0^{T/2} C(v_o(t))v_o(t)e^{-j2k\omega t}dt + \frac{1}{T}\int_{T/2}^{T} C(v_o(t))v_o(t)e^{-j2k\omega t}dt . \\ &= 0 \end{aligned} \tag{42}$$

C_{2k}=0 and V_{2k}=0 therefore satisfy the harmonic balance equations (38) and equation (40) is also a possible solution for the nonlinear differential equation (35). In the virtue of uniqueness, no even-order harmonic components exist in the output signal. Thus, it is confirmed there will be no even-order harmonic in an amplifier with odd-symmetry DC transfer in open-loop and closed-loop configurations.

IV. Conclusions

Because of the intrinsic nonideality of semiconductor devices, low-voltage, high-gain, open-loop amplifiers exhibit high nonlinearities. It always turns to be a confusing problem for circuit designers to make gain measurement and understand the non-ideality of close-loop configuration due to the nonlinearity of open-loop amplifiers. To solve this problem, a simple but effective model for nonlinear open-loop amplifiers is given, and the small-signal gain and large-signal gain are defined. Based on this model and the gain definitions, the nonidealities of feedback amplifiers with resistor networks for different considerations are inspected. Three equivalent gains are defined for different cases. An effective THD estimation method is given based on the definition of linear index. It is obvious that clarified gain definitions for nonlinear open-loop amplifiers help to identify the nonidealities of feedback amplifiers.

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CHAPTER 6 GENERAL CONCLUSIONS

The present work studied high-gain amplifier design using positive feedback techniques and focused on yield improvement. A CMOS amplifier was designed, fabricated, and measured to have high gain and high yield. Analysis, simulations and measurement results all confirmed this amplifier is suitable for very low-voltage, sub-100nm, digital CMOS processes. The use of nonlinear dynamical systems theory in positive feedback amplifier design was novel. The resulting bifurcation-detection methods were critical to achieving the desired robustness with respect to process variation, by enabling an all digital strategy for post process auto-tuning. Some adaptive calibration algorithms based on bifurcation were developed and analytical derivations suggested, and simulations confirmed, these algorithms would improve the positive-feedback amplifier's gain over processes, supply voltages, and temperature variations.

The present work also studied three layout techniques to improve one-to-one matching in IC processes. These new layout techniques are capable of canceling mismatch due to both linear and nonlinear gradients. The N^{th}-order circular symmetry and N^{th}-order central symmetry patterns, can cancel mismatches from linear to the n^{th}-order gradient between two devices by using 2^n unit cells for each one; the hexagonal tessellation pattern can cancel quadratic gradient with only 3 units for each device and has high area-efficiency. Among these three layout techniques, the N^{th}-order circular symmetry pattern has the best matching performance between 2 identical elements; central symmetry patterns have the best reported matching performance for Manhattan structures; the hexagonal tessellation pattern has high-density, high structural stability with its honeycomb structure. The N^{th}-order central symmetry technique is compatible with all IC fabrication processes requiring no special design rules. All layout patterns

have been mathematically proven and verified through simulation. Testing results confirmed excellent matching of the N^{th}-order central symmetry layout pattern.

Because high gain amplifier is one of the most fundamental building blocks for analog/mixed-signal circuits and systems, any progress in its design contributes to the evolution of integrated circuit design. Matching is one most critical property for circuits to achieve good performance. Without good matching, many circuits and systems will fall apart from performance. ITRS has predicted that it becomes more and more difficult for analog design and matching continues to deteriorate in the advanced CMOS processes. Our research results help to overcome part of these challenges. The present work provides a high gain amplifier capable operating in low-voltage digital CMOS, making it an important candidate for high performance analog/mixed-signal system-on-chips. The high gain amplifier can be used in high speed analog-to-digital converters, switched-capacitor filters and other analog-intense application. Our new layout techniques partly overcome or compensate matching degrading in the advanced processes thus help improve circuit performance. With our new layout strategies, it simplifies the work of designing high performance circuits. In addition to improving resistors' matching in our project, these techniques are universal to other devices' matching performance, either passive or active, in either integrated circuits or printed-circuits boards. Our new layout techniques can be utilized in all commercial/research fabrication processes which include CMOS, GaAs, InP and others. Beyond enhancing matching in IC fabrications, the matching techniques find applications in built-in tests, performance characterizations, instruments calibration, and so on.

Future research can be extended to adopt more researches from different fields into high performance circuit design, finding new applications for present work, study matching properties among arbitrary number of 'identical' devices and develop new techniques to enhance matching among multiple devices.